Boston University
College of Liberal Arts

Computer Science Department
111 Cummington Street, MCS 138
Boston, Massachusetts 02215
Tel: (617) 353-8919 / Fax: (617) 353-6457

CLA CS-550
Advanced Computer Architecture
Spring 1996

Instructor: Azer Bestavros

- **Office:** MCS-276
- **Office Hours:** Thu 11:00 – 12:30pm, or by appointments arranged through Email
- **Email:** best@cs.bu.edu
- **Phone:** 353-9726

Meeting Place: MCS B31

Meeting Time: Tue & Thu (9:30am – 11:00pm)

Web Home Page: `http://www.cs.bu.edu/faculty/best/crs/cs550`

Overview:

CS-550 overviews the concepts underlying the design of high-performance computer architectures, with an emphasis on quantitative evaluation and the interplay between computer architecture and the design of compilers and operating systems. Topics include: pipelined, superscalar, vector, and parallel processors; hard-wired scheduling and branch prediction; cache and virtual memory-hierarchy design; shared-memory and message-passing scalable multiprocessors. Case studies including RISC/CISC and SIMD/MIMD architectures. This course counts for 4 credits and assumes basic knowledge of computer systems.

Textbook and References:

- *Computer Architecture: A quantitative approach* John Hennesy and David Patterson, Morgan Kaufmann Publishers Inc., Second Printing 1990.
- *High-Performance Computer Architecture* Stone, Addison Wesley., Third Edition.
- *Computer System Architecture* Mano, Prentice Hall, Third Edition.
- *Advanced Computer Architecture: Parallelism, Scalability, Programmability* Kai Hwang, McGraw-Hill Series in Computing Science, 1993.
- *A collection of papers from various journals and conference proceedings – to be distributed.*

Class participation:

- ◇ Class participation is vital for a full understanding and appreciation of the material to be covered. This must be complemented with a consistent and thorough reading of the assigned portions of the textbook for a given lecture.

Homeworks and Tests:

- ◇ There will be a number of homeworks (≈ 6) spread out throughout the course. Some will be short and direct (one-week homeworks); others will be long and more like design projects (two-week homeworks).
- ◇ In addition to the homeworks there will be a final exam.
- ◇ The class grade will be based on homeworks (50%) and on the final exam (50%).

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Syllabus & Schedule

Class	Topic	Readings
1/16	First class meeting: Motivation and Overview	
1/18	Introduction: Key principles & terminology	Ch.1
1/23	Performance and Cost: Measures and Evaluation	Ch.2
1/25	Instruction Set Design: A review of basic principles	Ch.3
1/30	Instruction Set Design: Evaluation of alternatives	Ch.3
2/01	Instruction Set Design: Relationship with software technology	Ch.3
2/06	Instruction Set Design: Case Studies (VAX, IBM 360/70, 8086 & DLX)	Ch.4
2/08	Processor Design: Building blocks	Mano
2/13	Processor Design: From N-P Junctions to Logic Circuits	
2/15	No Class. (Substitute Monday)	
2/20	Processor Design: Datapath and Control	Ch.5
2/22	Processor Design: Hardwired and Microprogramming control	Ch.5
2/27	Pipelining: Introduction and concept	Ch.6
2/29	Pipelining: Basic designs	Ch.6
3/05	Spring Recess	
3/07	Spring Recess	
3/12	Pipelining: Dynamic scheduling & Parallelism	Ch.6
3/14	Pipelining: Dynamic scheduling & Parallelism	Ch.6
3/29	Pipelining: Advanced concepts	Ch.6
3/21	Superscalar and Vector Processing	Ch.7
3/26	Memory-hierarchy design: Basic concepts	Ch.8
3/28	Memory-hierarchy design: Caching	Ch.8
4/02	Memory-hierarchy design: Main and virtual memory	Ch.8
4/04	Input/Output and Networks	Ch.8
4/09	ALU Design: Efficient Hardwired Algorithms	
4/11	Parallel Processing: Introduction	Ch.10
4/16	Parallel Processing: Interconnection Topologies	Hwang
4/18	Parallel Processing: Shared Memory Architectures	Hwang
4/23	Parallel Processing: Latency Hiding Architectures	Hwang
4/25	Parallel Processing: Dataflow Architectures	Hwang
4/30	Conclusion	
5/07	Final Exam	

** Changes to this schedule will be announced if need be.*