Wide Dynamic Range, Low Power Dissipation

Optical Preamplifier

for

Wireless Infrared and LAN Communications

by

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ABSTRACT

The challenge of creating inexpensive links for wireless infrared and optical local area networks (LANs) is driving new innovations in the design of optical transceivers. The low-cost, ad hoc nature of these links means that low power dissipation and wide dynamic range are critical design requirements for the preamplifier stage of the receivers.

To meet these requirements, this thesis presents and compares four new preamplifier topologies. We first develop a means of varying the gain of a traditional preamplifier via non-linear clamping. We then devise methods to allow the traditional preamplifier to process signal currents on the order of its bias currents. To this end, we introduce a shunting technique that limits the photocurrent flowing into the amplifier, as well as two topologies that dynamically vary the preamplifier bias currents according to signal conditions.

ACKNOWLEDGEMENTS

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For my grandfather.

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1 INTRODUCTION

1.1 Overview

The benefits of optical communication, traditionally used to increase the capacity of long-haul networks, are now being brought closer to the end user through technologies such as optical local area networks (LANs), and wireless infrared (IR) communication. Optical LANs use fiber as the physical transmission medium for networks serving resources within a small geographic area, while wireless IR uses free space as a communication channel for short-range, localized networks. Optical communication can bring the benefits of high-speed transmission and isolation from electromagnetic interference to a variety of diverse applications.

Current optical LANs, represented by the Gigabit Ethernet and ATM-PON network specifications, can be used to realize high data rate systems that find their applications in parallel processing environments, newspaper and magazine production, and medical imaging networks [Kazovsky, 2000]. The immunity of fiber optic LANs to electromagnetic radiation makes this technology an attractive choice for implementation in sensitive environments such as aircraft [Andersen, 1998]. Furthermore, broadband requirements for that connect central office locations to customer premises benefit from the high bandwidths made feasible through the use of fiber-to-the-home (FTTH) technology. Today, the limiting factor in the deployment of advanced optical LANs is the prohibitive cost of the technology, including the costs of the emitter and receiver [Kim, 1997]. However, novel integrated circuit design techniques are helping drive down the cost of implementation, making these LAN solutions more common.

Wireless IR is an attractive means of communication for next-generation free-space serial links and LANs, where portability and low cost are a priority. The IR medium is unregulated. Moreover, IR signals cannot propagate through opaque obstructions so that signals can be confined to the room in which they are transmitted, reducing the possibility of interference. These benefits, coupled with the fact the IR range is in the peak wavelength region of low-cost silicon LEDs, makes this medium an attractive one for short range, indoor, low-cost transmission. Applications of wireless IR include connecting portable devices, like PDAs, laptops, digital cameras and even cell

phones to a wired LAN backbone or a computer peripheral like a printer. Wireless IR can also be used to establish a directed serial link between two portable devices, such a laptop computer and PDA.

A typical optical link is shown in Figure 1.1. The data stream is generated by an information source, which is then modulated and sent to the emitter drive circuitry as a digital signal. An LED or laser then sends data through free space or optical fiber channel to a receiver. At the receiver, a photodetector converts the optical signal to a photocurrent (i_{PD}) that is sensed by the preamplifier. The preamplifier then regenerates and converts the signal to a voltage that the demodulator uses to recover the data, which is sent downstream for further processing.

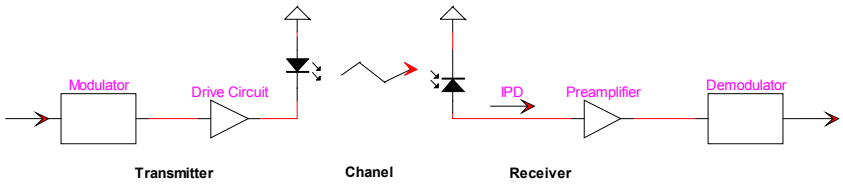


Figure 1.1 Optical communication link.

Varying link lengths are driving new innovations in the design of transmitter and receiver technology for optical communication systems. For wireless LAN technologies, end users may located be a short distance away from each other, while others could be on different floor or in another building. The ad hoc nature of these networks necessitates the use of varying link lengths. This is exemplified in the optical LAN network specifications; a 10 Gigabit Ethernet standard link length, for example, can vary between 2m to 300m[1]. Moreover, the IrDA[2] has established standards for wireless IR links that specify that receivers must resolve signals transmitted over link distances that can vary, at minimum, between zero and one metre. Because photocurrent amplitude is directly proportional to received signal intensity, this range of channel distances translates to a preamplifier signal current that can vary through five orders of magnitude [Phang, 2001].

Furthermore, for inexpensive free space links, the IrDA has specified system bandwidths of up to 16Mbps. Optical LANs operate at higher speeds, with 100Mbps or

[1] For 50 micron multimode fiber with modal bandwidth 2000 MHz*km for the 10 Gigabit Ethernet standard
[2] IrDA - Infrared Data Association

1Gbps networks commonly in use today [Spurgeon, 2002]. As inexpensive optical links become widespread, the low cost and high potential for integration of CMOS technology has made it a popular choice for realizing receivers.

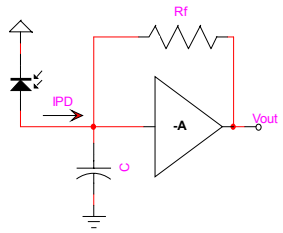


Figure 1.2 Basic preamplifier topology

For the preamplifier in particular, CMOS transimpedance amplifiers have become a popular choice for realizing photocurrent sensing and amplification. Transimpedance amplifiers can be used to achieve the wide bandwidth and dynamic range necessary in these applications. The basic topology of a transimpedance amplifier is shown in Figure 1.2, where *C* is the total capacitance at the input node as a result of the amplifier and photodetector. Feedback creates wide bandwidths by reducing the effective resistance seen by the photodetector by a factor of *(1+A)*. The closed loop transimpedance gain of the preamplifier is then given by

$$\frac{v_{out}}{i_{PD}} = -\frac{A}{1+A} R_f \approx -R_f \qquad (1.1)$$

so that the transimpedance gain is determined by the value of the feedback resistance.

1.2 Design Goals and Specifications

This chapter describes the photodetector model used for simulation purposes as well as three major design goals which guide the design of the topologies presented in this thesis: low power dissipation, wide dynamic range and bandwidth.

1.2.1 Photodetector model

A photodetector is a device that converts incident light into an electric photocurrent. Low cost communication links favour the use of photodiodes to detect optical signals because of their low cost, good frequency response and potential for

integration with on-chip CMOS circuitry. When light is incident on a reverse-biased photodiode, a reverse photocurrent will be generated that is directly proportional to the intensity of the incident light.

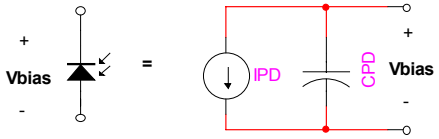


Figure 1.3 Photodetector equivalent circuit.

In this thesis, we model the activity of the photodiode using the equivalent circuit shown in Figure 1.3 [Sackinger, 2002]. i_{PD} models the photocurrent generated by the detector, which for digital communication systems, can be represented by a square wave that takes on either zero or some positive value. The photodiode parasitic capacitance is modeled by C_{PD}. While current designs assume a C_{PD} that ranges from 10pF or 0.5pF or less, here we assume a relatively large photodetector capacitance of C_{PD}=5pF.

1.2.2 Wide Dynamic Range

Because wireless IR networks and optical LANs use links of varying length, preamplifiers must be designed to contend with a wide dynamic range of input photocurrent signals. Today, the low-cost free-space links specified by the IrDA requires the receiver preamplifier to process input photocurrents that can vary through five orders of magnitude, or 100dB. Additionally, the ad hoc nature of optical LANs, where fiber link length can vary, mean that it is critical the receiver be able to function with both strong and weak signals. It is the primary goal of this thesis to study ways to increase the dynamic range of the transimpedance preamplifier.

Designs reported to date ([Yamakazi, 1997], [Ohhata, 1999]) set the upper limit on input photocurrent at about 1 or 2mA. With this upper limit, a circuit with a dynamic range of about 100dB must be able to handle photocurrents ranging from 20nA to 2mA. However, because noise analysis[3] is considered outside the scope of this work, we are mostly interested in increasing the upper limit of the preamplifier dynamic range while ensuring stability under small signals.

[3] Noise analysis is to determine the lower input signal limit of a design.

1.2.3 Low Power Dissipation

An important method of driving down receiver cost is reducing power dissipation. Thus, while it is possible to increase the dynamic range of the preamplifier by simply increasing bias current levels, this thesis investigates other methods to achieve a wide dynamic range. The topologies presented here, suitable for low-power, low-cost applications, are designed to achieve a power dissipation comparable to that of a traditional preamplifier with a dynamic range of approximately 200μA, and a power dissipation of 3.96 mW (single-ended output) or 5.28 mW (fully-differential output).

1.2.4 Wide Bandwidth

One of the challenges of designing circuits in CMOS is achieving wide bandwidths with low-cost technology. For logistical reasons, this thesis assumes a that 0.35 micron fabrication technology will be used to realized the designs described here, which may be considered a slow technology when compared to 0.25 or 0.18 micron technologies available today. Since the goal of this thesis is to investigate and compare novel topologies that increase dynamic range, little time is spent optimizing individual circuits to improve bandwidth. Therefore, although the designs present here are slower than many of the designs reported today, our topologies may be optimized and fabricated in faster processes in order to achieve higher data rates.

The circuits designed in this thesis achieve data rates of about 50Mbps, which can are sufficient for use in the low cost IR links specified by the IrDA, or 10Mbps Ethernet standards. Higher speed applications, like optical LAN networks operating in the 1Gbps range, require that the circuits described here be optimized for wider bandwidth. However, most of the designs presented in this work are not suitable for data rates above 1Gbps, because of differences in the signal paths or complexities introduced by extra feedback loops.

1.3 Review of Transimpedance Amplifier Designs

The challenge of designing a transimpedance amplifier with wide dynamic range has been tackled in a number of ways. Traditional designs have used variable feedback resistors to implement a variable gain transimpedance amplifier. A popular scheme uses

MOS transistors biased in the triode region that vary their output resistance according to a control voltage determined from an external feedback loop. (see [Cura, 2001], [Khorrmabadi, 1995], [Meyer, 1994] or [Yamashida, 2002]). An alternative method involves using an array of pass transistors that can switched on or off according to a control voltage to realize a finite set of resistances [Phang, 2001]. Both methods require careful tuning of the control voltages, as well as the addition of an extra feedback loop that senses the preamplifier output voltage levels and adjusts control voltage accordingly. Another approach, [Hayes, 2002], uses the nonlinear characteristics of a bipolar transistor to realize a transimpedance amplifier with a logarithmically varying transimpedance. This thesis presents a new gain variation approach through the use of diode clamping.

However, varying the gain of the preamplifier does not change the fact that under strong signals the system must still absorb large currents. If bias currents are kept small in order to decrease power dissipation, dynamic range is limited since the preamplifier cannot handle photocurrents greater than larger than its bias currents. This problem cannot be avoided even if the gain is drastically reduced.

An alternative scheme for increasing dynamic range involves using limiting to reduce the gain of the transimpedance amplifier. Limiting has been preformed after to the amplifier, [Nakamura, 1999], [Ohhata, 1999]. However, this type of external limiting cannot improve the preamplifier's ability to recover from large currents. Alternatively, if limiting is preformed internally by reducing the magnitude of the signal current injected into the transimpedance amplifier [Yamakazi, 1997], then the preamplifier can be made to handle larger input currents without affecting its performance under small input signals. The upcoming chapters will discuss a method for implementing this internal limiting technique though the use of current shunting, as well as novel dynamic biasing techniques that compensate for the detrimental effects of large signal currents by adjusting amplifier bias currents.

1.4 Thesis Outline

This thesis presents and compares three techniques that can be used to optimize the dynamic range of an optical preamplifier without significantly increasing power dissipation. Chapter 2 presents of two traditional transimpedance amplifier designs and

discusses their limitations. To address some of these limitations, in Chapter 3 we introduce a clamping technique for realizing a nonlinear variable transimpedance amplifier. We then study methods of enabling the preamplifier to handle photocurrents on the order of its bias currents. Chapter 4 describes a shunting design that can be used to limit the photocurrent flowing into the preamplifier. In Chapter 5 we focus on methods to dynamically vary bias currents. Our conclusions are presented in Chapter 6.

2 BACKGROUND

2.1 Conceptual Circuit Topology

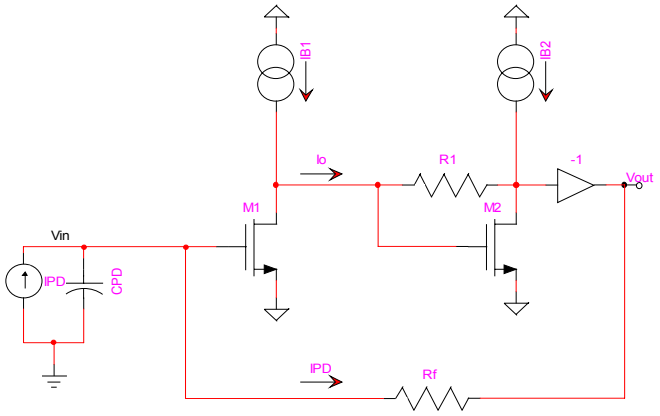


Figure 2.1 Traditional transimpedance amplifier conceptual circuit topology

Figure 2.1 shows the conceptual topology of a traditional transimpedance amplifier. The transimpedance amplifier comprises a resistor in feedback across a voltage amplifier, as in Figure 1.2. The voltage amplifier consists of a transconductance stage followed by an internal transimpedance stage. The internal transimpedance stage is a common source amplifier with resistor R_1 in feedback. The use of an internal transimpedance stage similar to the overall topology of the circuit means the voltage across R_1 will track the voltage across R_f. This allows for excellent matching between these two resistors, which will be shown to be critical to ensuring the stability of the preamplifier. The internal transimpedance stage is preceded by transconductance stage using another common source amplifier. Finally, the negative gain of the voltage amplifier, -A, is achieved via small signal inversion after the transimpedance stage. The overall gain of the voltage amplifier is given by

$$\frac{v_{out}}{v_{in}} = -A = -g_{m1}R_1 \frac{(R_1 \| r_{ds1})(R_1 \| r_{ds2})(g_{m2}R_1 - 1)}{(R_1 \| r_{ds1})(R_1 \| r_{ds2})(g_{m2}R_1 - 1) - R_1^2} \cong -g_{m1}R_1 \qquad (2.1)$$

2.1 Stability

To analyze the stability of this circuit, we break the loop at the input node. Because the photodetector capacitance dominates all other capacitances in the circuit, the

inverse product of R_f and C_{PD} gives the dominant pole in the open loop. The unity gain frequency of the loop is

$$\omega_t \cong \frac{A}{R_f C_{PD}} \cong \frac{g_{m1} R_1}{R_f C_{PD}}. \qquad (2.2)$$

The internal parasitics of the voltage amplifier determine the second pole frequency. The second pole may be determined using the small signal model given in Figure 2.2, where C_i is the capacitance at the internal node, C_o is the capacitance at the output node, and C_f is the gate-drain capacitance of transistor M_2. As shown in [Phang, 2001], if assume that g_{m2} ™ $1/r_{ds2}$ and R_1 , and that $C_f \vee C_i$ and C_o, we obtain the following transfer function

$$\frac{v_{out}}{v_{in}}(s) = -\frac{g_{m1}}{C_i C_o} \frac{sC_f + (1/R_1 - g_{m2})}{s^2 + \frac{g_{m2} C_f}{C_i C_o} s + \frac{g_{m2}}{C_i C_o R_1}} \qquad (2.3)$$

We can tune C_f to make the poles of the transfer function complex, pushing them as far way from ϖ_t as possible. Thus, our second pole frequency is given by a set of complex poles characterized by

$$\omega_o = \sqrt{\frac{g_{m2}}{C_i C_o R_1}} \quad \text{and} \quad Q = \frac{1}{C_f} \sqrt{\frac{C_i C_o}{g_{m2} R_1}} \qquad (2.4)$$

so that the amplifier can made stable, with adequate phase margin, if we design $\omega_o \approx 2\omega_t$.

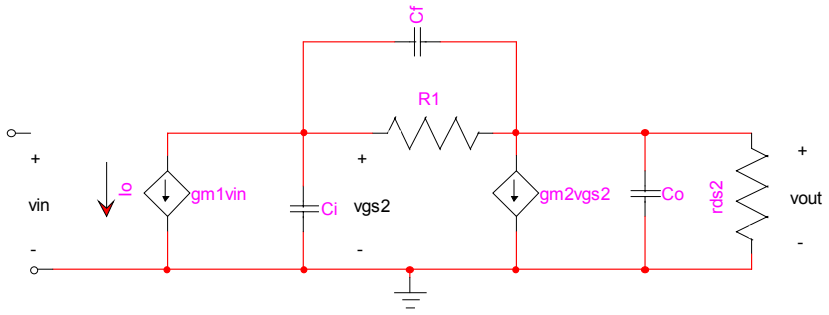


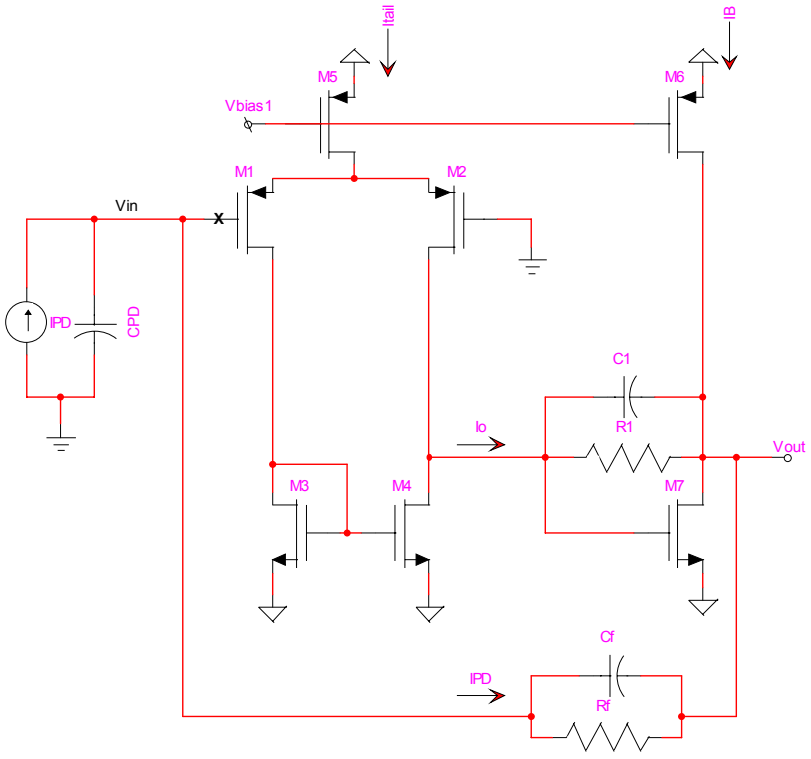
Figure 2.2 Small signal model used for frequency analysis of the traditional amplifier

From equations 2.2 and 2.4 we can see that ω_t increases as R_f decreases, while ω_o remains fixed relative to changes in R_f. Since the stability of this system is determined by the relative position of ω_t and ω_o, this threatens the stability of the amplifier when the transimpedance gain is reduced. However, we can remedy this problem by making R_1

track R_f, so that as the transimpedance gain decreases, the unity gain frequency remains constant while second pole frequency increases, assuring the stability of the amplifier.

2.2 Single-Ended Design

A differential-input, single-ended output topology based on the conceptual circuit presented in the previous section was designed according to [Phang, 2001]. Using a differential input improves rejection of noise at the input, while allowing us to realize small signal inversion through cross-coupling. The details of the design are given in Figure 2.3 below.



CMOS .35µm	
R_1	5 kΩ
R_f	5 kΩ
C_{PD}	5 pF
C_1	60 fF
C_f	60 fF
M_1	24x8/0.5
M_2	24x8/0.5
M_3	12x10/1.2
M_4	12x10/1.2
M_5	20x20/1.2
M_6	10x20/1.2
M_7	6x10/0.6
V_{DD}	2.52 V
V_{SS}	-0.78 V
I_B	400 µA
I_{TAIL}	800 µA

Figure 2.3 Single-ended transimpedance amplifier topology and design details.

The frequency response of the circuit, when we break the loop at point X, is shown in Figure 2.4. We can see that when R_f = 5kς the system is stable with a phase margin of 758 at a unity gain frequency of 73MHz.

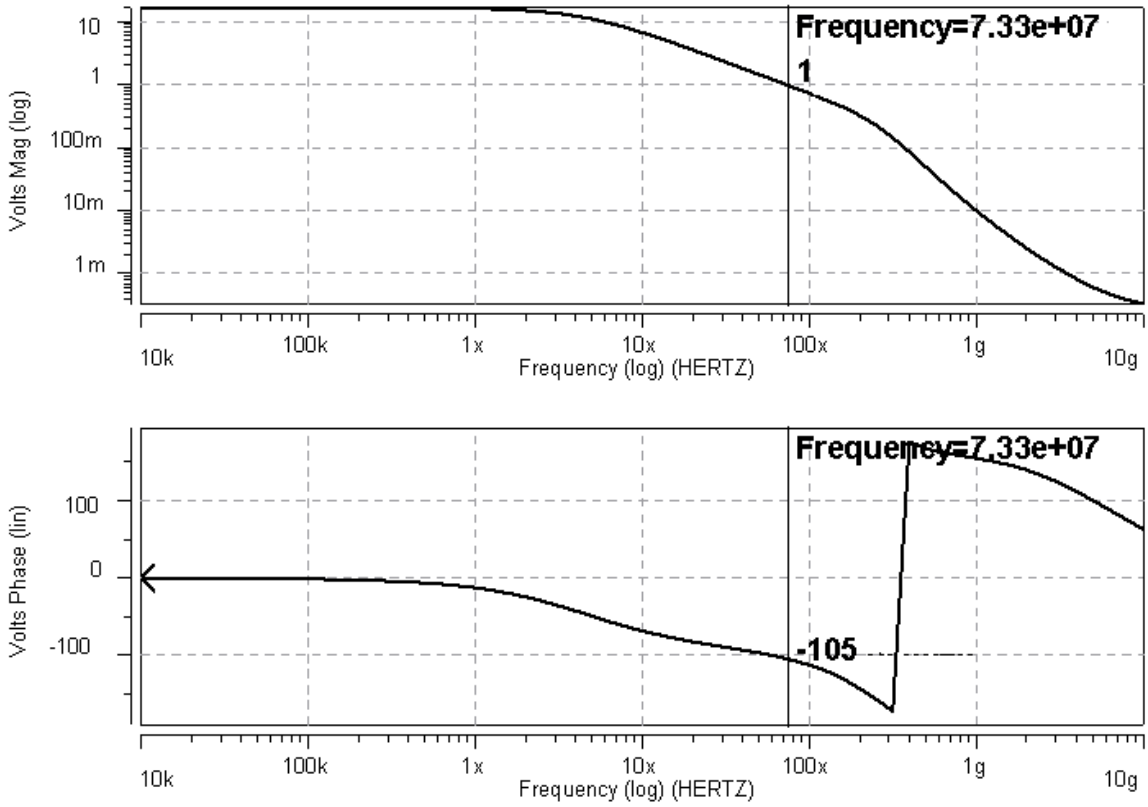


Figure 2.4 Open loop frequency response of single-ended preamplifier. The preamplifier is stable with a phase margin of 758 at a unity gain frequency of 73MHz.

2.3 Fully Differential Design

The improved noise rejection capability realized through the use of fully differential amplifiers make them a attractive choice for optical receiver design, where high signal to noise ratios are extremely important. A fully differential version of the transimpedance amplifier [Phang, 2001] is presented in Figure 2.5. All sizing is as given in Figure 2.3. The open-loop frequency response of the circuit when the loop is broken at X, is given in Figure 2.6, from which we can see that the amplifier phase margin of the circuit is 80.5° at a unity gain frequency of 75MHz. The practical maximum limit on the input photocurrent is about 170μA, for reasons described below.

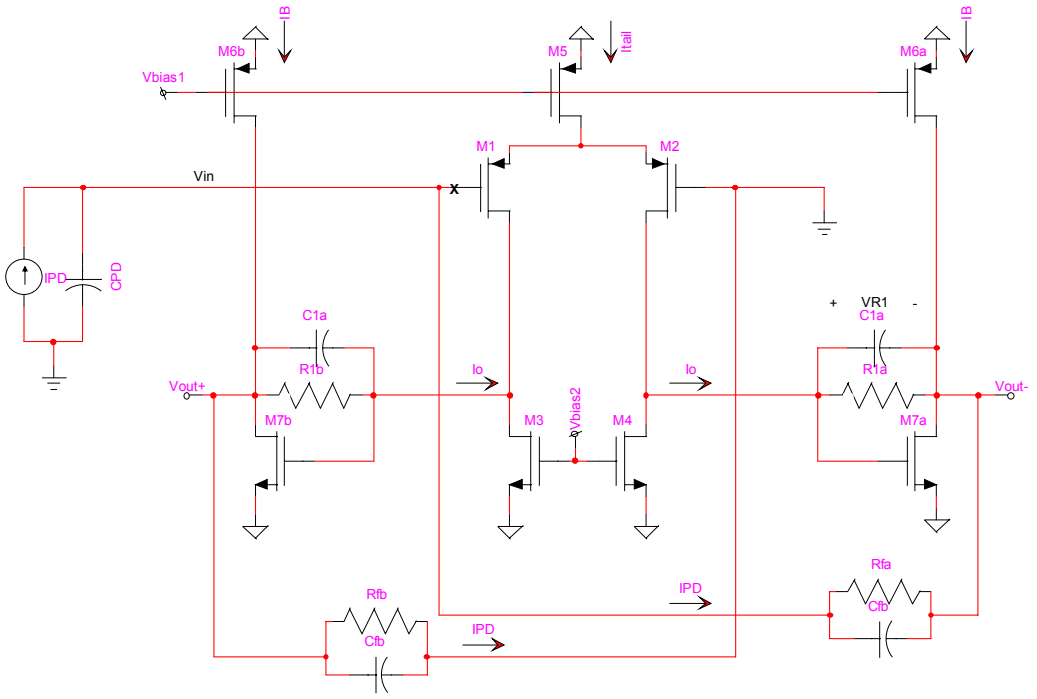


Figure 2.5 Fully-differential design topology.

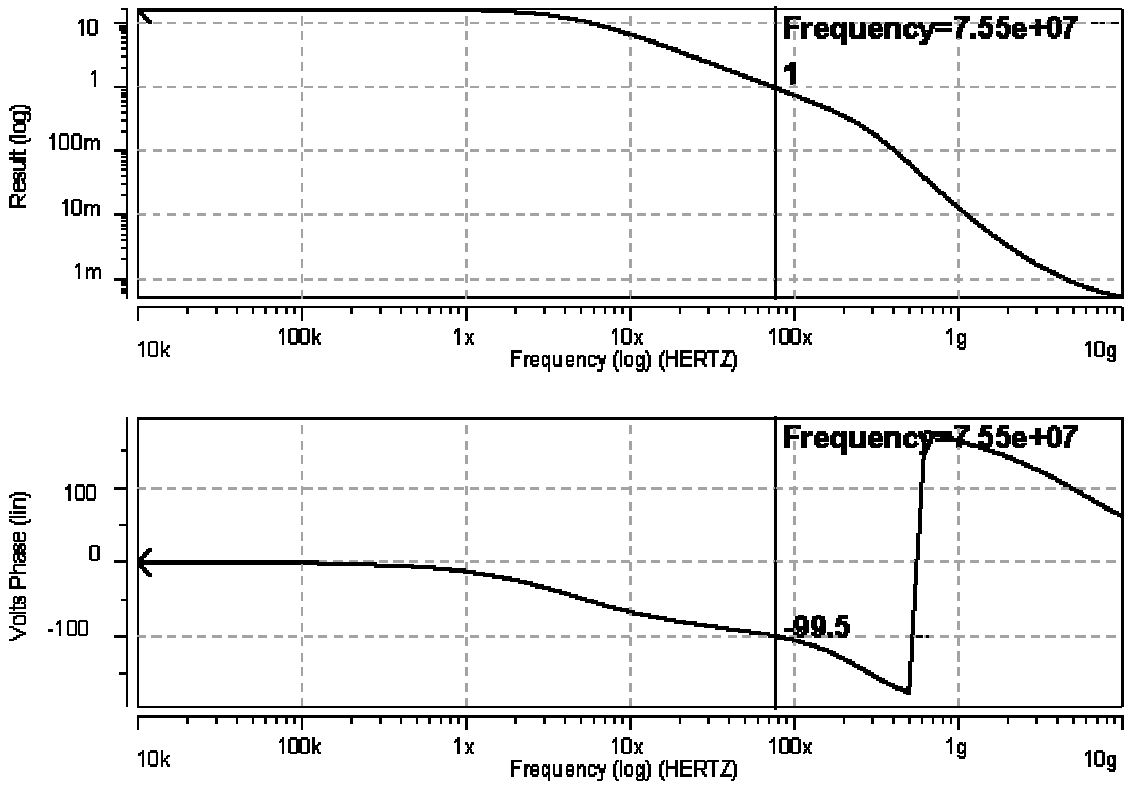


Figure 2.6 Frequency response of fully differential amplifier.

2.4 Limitations of the Traditional Design

One of the major goals of this thesis is to improve the traditional preamplifier's ability to absorb large signal currents, where, in this thesis, "large signal currents" are defined as signals that are on the order of the currents used to bias the circuit. Unfortunately, the traditional preamplifier circuit described above has a number of shortcomings that prevent it from functioning properly under large signals. These problems, described below, are most acute at the internal transimpedance amplifier stage.

2.4.1 Second Stage Transistor Entering Triode

From Figure 2.3, which indicates the direction of signal current flow in the single-ended amplifier, we can see that the current generated by the internal transconductance stage, i_o, is given by

$$i_o = -g_{m1} v_{in} \quad [4] \qquad \textbf{(2.5)}$$

While, from equation 2.1, the output of the second stage is given by,

$$v_o \cong R_1 i_o \qquad \textbf{(2.6)}$$

Applying equation 1.1, we find that i_o mirrors i_{PD} because

$$i_o \cong \frac{R_f}{R_1}\frac{A}{A+1} i_{PD} \cong i_{PD} \qquad \textbf{(2.7)}$$

when $R_f = R_1$.

Furthermore, if we assume that M_7 enters the triode region when $v_{gs7} > V_{eff7}$, then for M_7 to remain in the active region, the voltage across R_1 must always exceed the transistor threshold voltage. In other words

$$v_{R1} = i_o R_1 \cong i_{PD} R_1 > V_{tn} \qquad \textbf{(2.8)}$$

Thus, when

$$i_{PD} > \frac{V_{tn}}{R_1} \qquad \textbf{(2.9)}$$

[4] The negative sign arises because we take to output on the opposite side of the differential pair.

M_7 enters the triode region, reducing the gain of the voltage amplifier and slowing down its recovery time from large input current pulses.

2.4.2 Second Stage Transistor Entering Cutoff

Examining the direction of signal current flow in Figure 2.5, we can see that both i_{PD} and i_o are drawn out of M_{7b}. However, under large signals the sum $i_{PD} + i_o$ may be larger than the current used to bias M_{7b}, causing this transistor to enter to cutoff region. This is a serious problem that completely destroys the gain of the voltage amplifier. Furthermore, after large input signal current is injected into the circuit, there long recovery time during which the output voltage returns to its quiescent value as M_7 leaves the cutoff region. As shown previously, i_o mirrors i_{PD} so that we obtain the important relationship

$$i_{PD}^{\max} > \frac{I_B}{2} \qquad \textbf{(2.10)}$$

which sets upper limit on the dynamic range of the traditional transimpedance amplifier. For the fully-differential topology presented in [Phang, 2001], the practical maximum signal current is l70μA, with is slightly less than the maximum set by I_B=400μA.

3 THE CLAMPING DESIGN

3.1 Motivation

A diode clamping technique can be used to implement a variable-gain transimpedance amplifier with a non-linear gain characteristic. Additionally, in order to prevent the internal transimpedance drive transistor (M_7) from leaving the active region, the voltage across the internal feedback resistor R_1 must not exceed V_{tn} (see section 2.4.1). One way to reduce the voltage drop across the internal feedback resistor is to add a diode across R_1 that will shunt currents away from R_1. Furthermore, as mentioned in section 2.1, in order to maintain the stability of amplifier, R_1 must track changes in R_f. To fulfill this requirement, identical diode clamps are added across both feedback resistors.

3.2 Implementation

Figures 3.1 and 3.2 show the clamping scheme used in both single-ended and fully-differential designs.

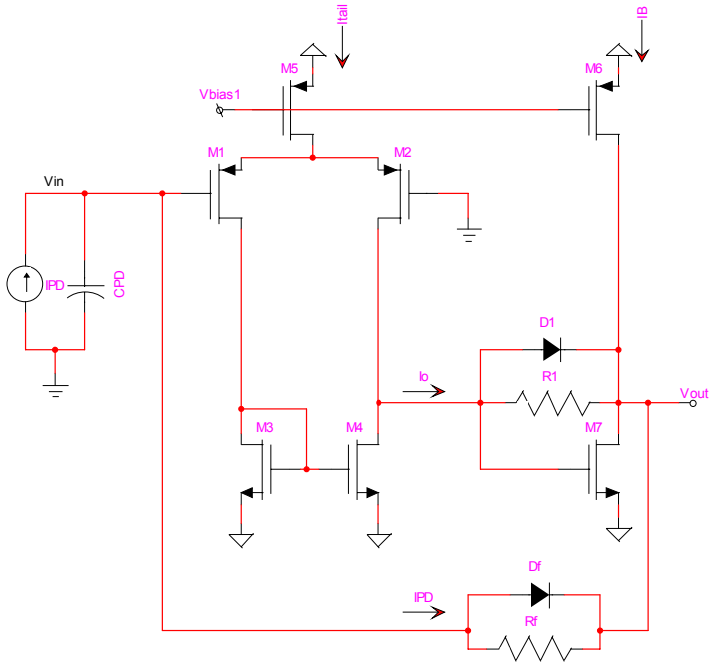


Figure 3.1 Single-ended output clamping topology.

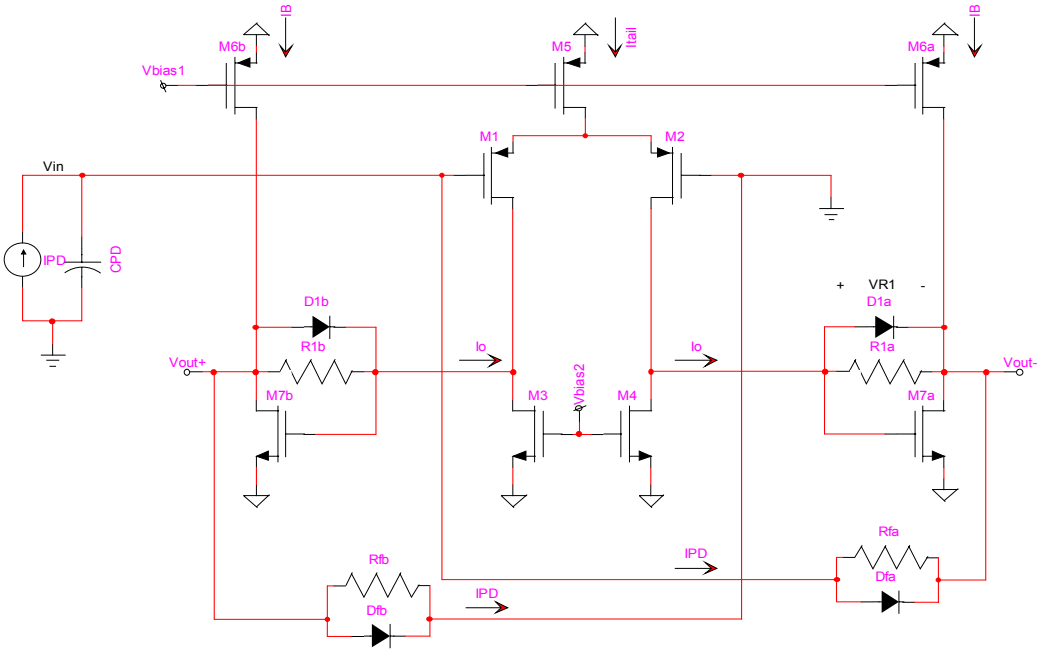


Figure 3.2 Fully-differential output clamping topology.

Because the photocurrent can only take on zero or positive values, signal currents flow in the circuit only in the manner shown in the figure. As such, we can install the diode clamps in the amplifier in the asymmetrical fashion shown.

The amplifier topology presented here is well suited to this clamping scheme. Because the voltages at the input and the internal node are approximately equal and have a relatively small signal swing, the two clamps have almost the same voltage drop across them at all times. Thus, to a first order approximation, D_1 and D_f will shunt excess currents so that R_1 and R_f will have equal currents flowing through them at all times. In this way, we meet the requirement that R_1 tracks R_f.

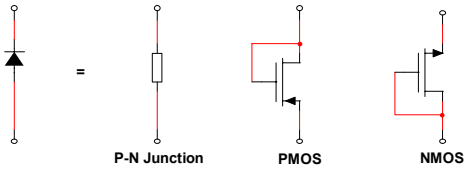


Figure 3.3 Possible realizations of the diode clamp.

A variety of different methods can be used to implement the diodes, as shown in Figure 3.3. One possibility is the p-n junction diode. The p-n junction has small signal resistance and capacitances that are highly dependent on the voltage across the junction.

These large varying impedances will cause decreases and volatility in the system bandwidth, making them an impractical solution for this application.

Another option is to use a diode-connected MOS transistor. With this approach, the bandwidth is about three decades wider than bandwidth of a system using p-n junction clamps. However, the diode will follow a square law I-V characteristic rather than the more desirable exponential characteristic obtained from a p-n junction. The threshold voltage of the NMOS diode, V_{tn}, is lower than the threshold voltage of the PMOS, $|V_{tp}|$. Because we must ensure the gate-drain voltage of the internal transimpedance drive transistor (M_7) is less than V_{tn}, NMOS diodes are the most logical choice.

3.3 Design Details and Simulation Results

We can control the steepness of the NMOS diode I-V characteristic by increasing the width of the diode-connected transistor. However, doing this also increases the capacitance between the output and internal node, which can threaten the stability of the system (see Section 2.1). Thus, the NMOS diode sizing was chosen as (50/.5), as compromise between these two requirements. The sizing for the rest of the design is as given in Figure 2.3.

Because the single-ended topology we are not limited to input currents less than $\frac{1}{2}I_B$ (see section 2.4.2), this topology is used to study the performance of the clamping scheme. The analysis for the fully-differential design is very similar, apart from a common mode rejection issue that will be raised in the following discussion.

3.3.1 Tracking between feedback resistors

Figure 3.4 shows a sweep of currents through the feedback resistors for increasing photodiode currents. These currents grow linearly until they are limited to about 100μA, when the diodes turn on and begin shunting away a portion of the signal current. From Figure 3.5, tracking between currents in the feedback resistors in the transient response is readily observed.

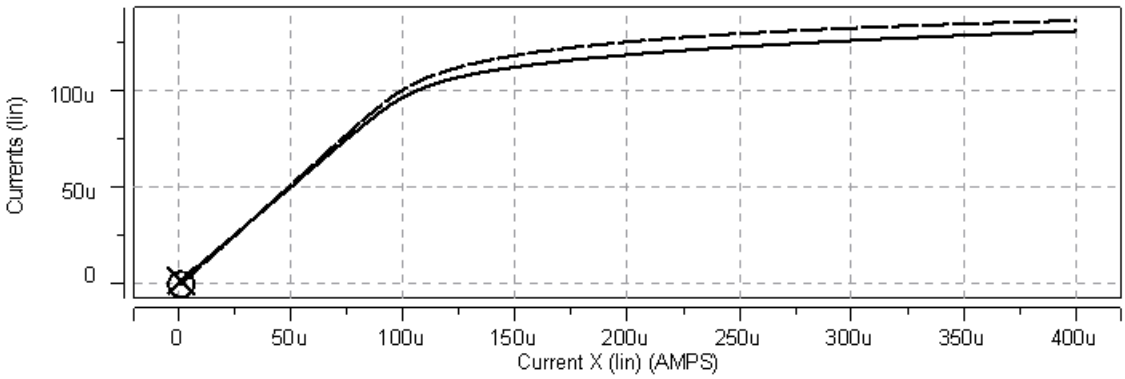


Figure 3.4 Sweep of currents in feedback resistors versus increasing photocurrent.

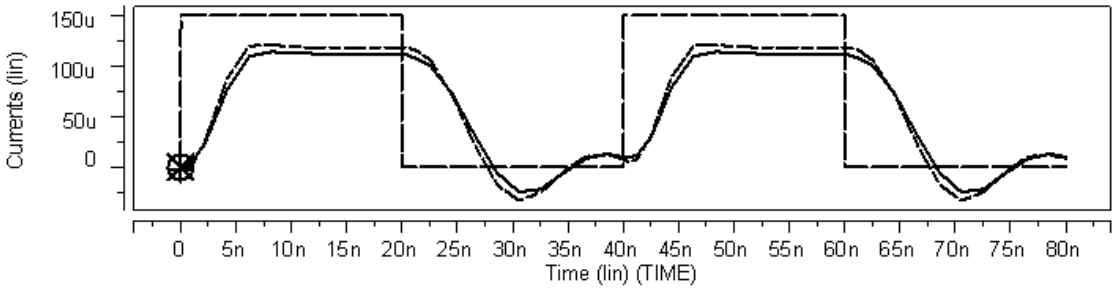


Figure 3.5 Transient currents through feedback resistors. 150µA photocurrent input.

3.3.2 Limiting of Output Voltage

Figure 3.6, a sweep of the voltage at the output node versus photocurrent, indicates that when the clamps begin to take effect, the output voltage is limited to just under $V_{eff\,7}$ for the second stage drive transistor. Additionally, despite the fact that the voltages across the feedback resistors (the signal voltages) are clamped, the output voltage increases slowly after clamping has begun. This occurs because the large current signals absorbed in M_7 drive up the voltage at the output node.

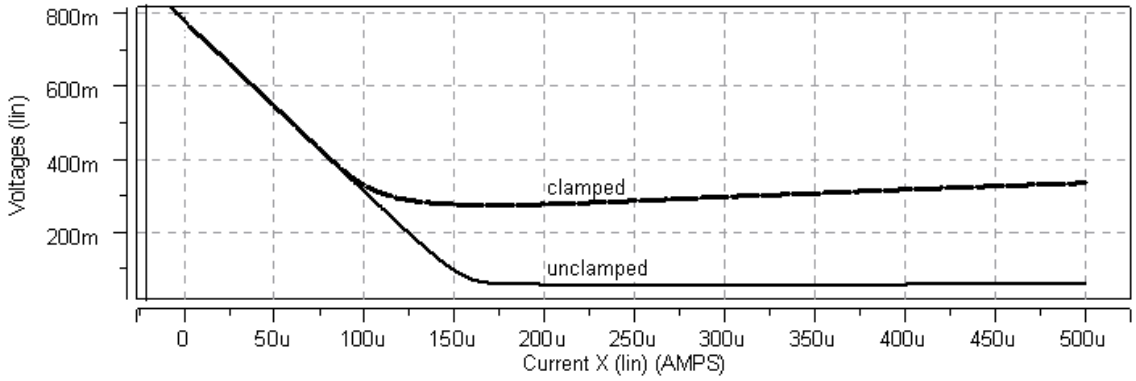


Figure 3.6 Output voltage versus increasing photocurrent for clamped and unclamped topologies.

3.3.3 Transients

Figure 3.7 compares the transients for the single-ended amplifier using both a clamped and an unclamped topology. In the small signal regime, the clamps have little effect on the response of the system, as show from the 3μA example. For the 150μA example, the output voltage in the clamped case has been limited to about 300mV, as compared to the unclamped case, where transistor M_7 is well into the triode region and the output voltage has dropped almost to zero. The delay in the recovery time of the 300μA unclamped transient is the result of this transistors descent into the triode region. The capacitance of the diode has slightly degraded the small signal step response by increasing rise time and overshoot, but with careful design these effects can be minimized.

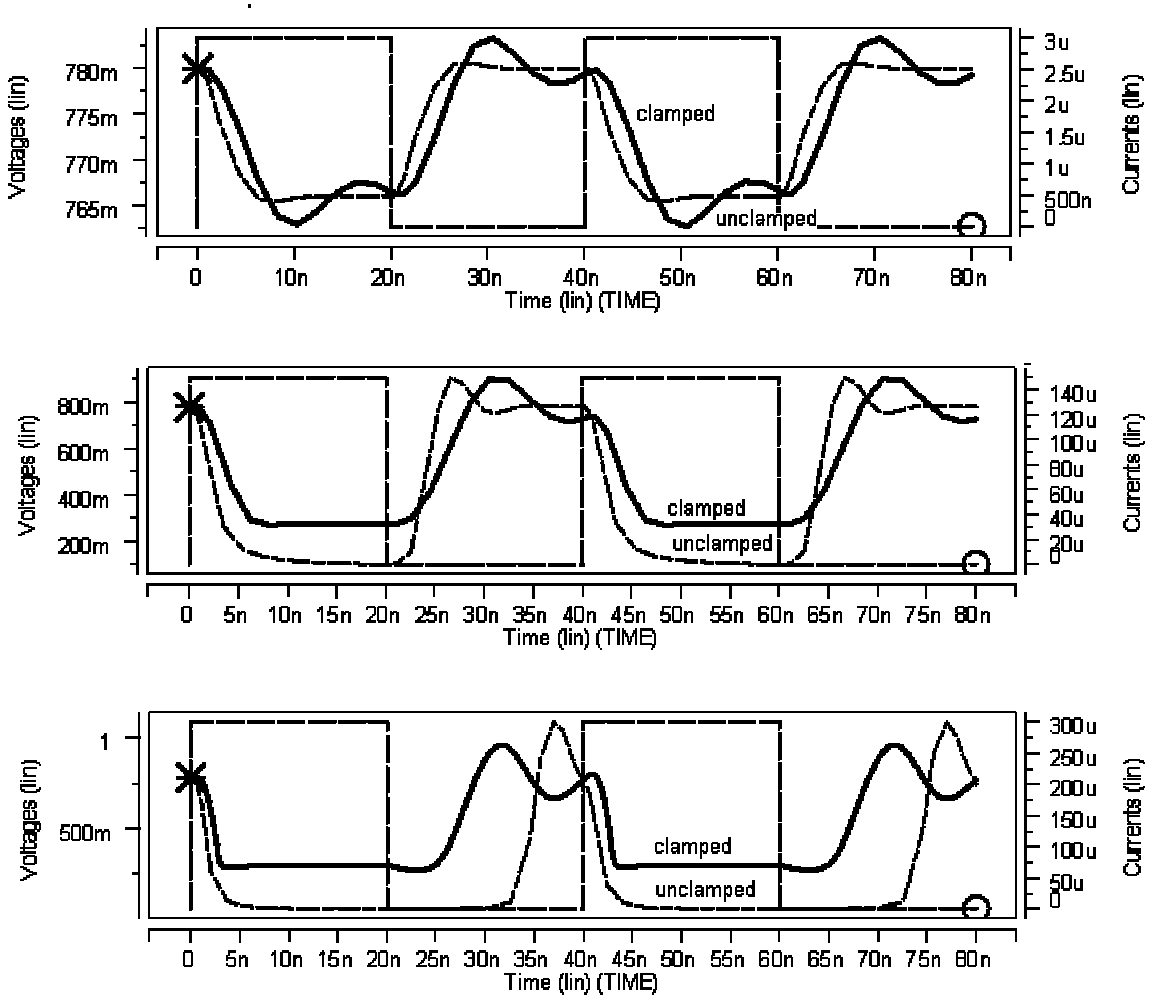


Figure 3.7 Output voltage transients for 3uA, 150uA, and 300uA photocurrents for clamped and unclamped topologies.

3.3.4 Common Mode Rejection

If we restrict our study of the fully differential design to photocurrents less than $\frac{1}{2}I_B$, an interesting effect is observed. For relatively large input signal currents, clamping has forced the currents flowing in R_1 and R_f to track in each individual half circuit,. However, under relatively large signals, the voltages at nodes on either side of the amplifier are different. This will prevent the currents flowing in resistors on different sides of the differential amplifier (i.e. R_{fa} and R_{fb}) from tracking perfectly, resulting in a non-zero steady-state common mode signal. Figure 3.8 illustrates this concept.

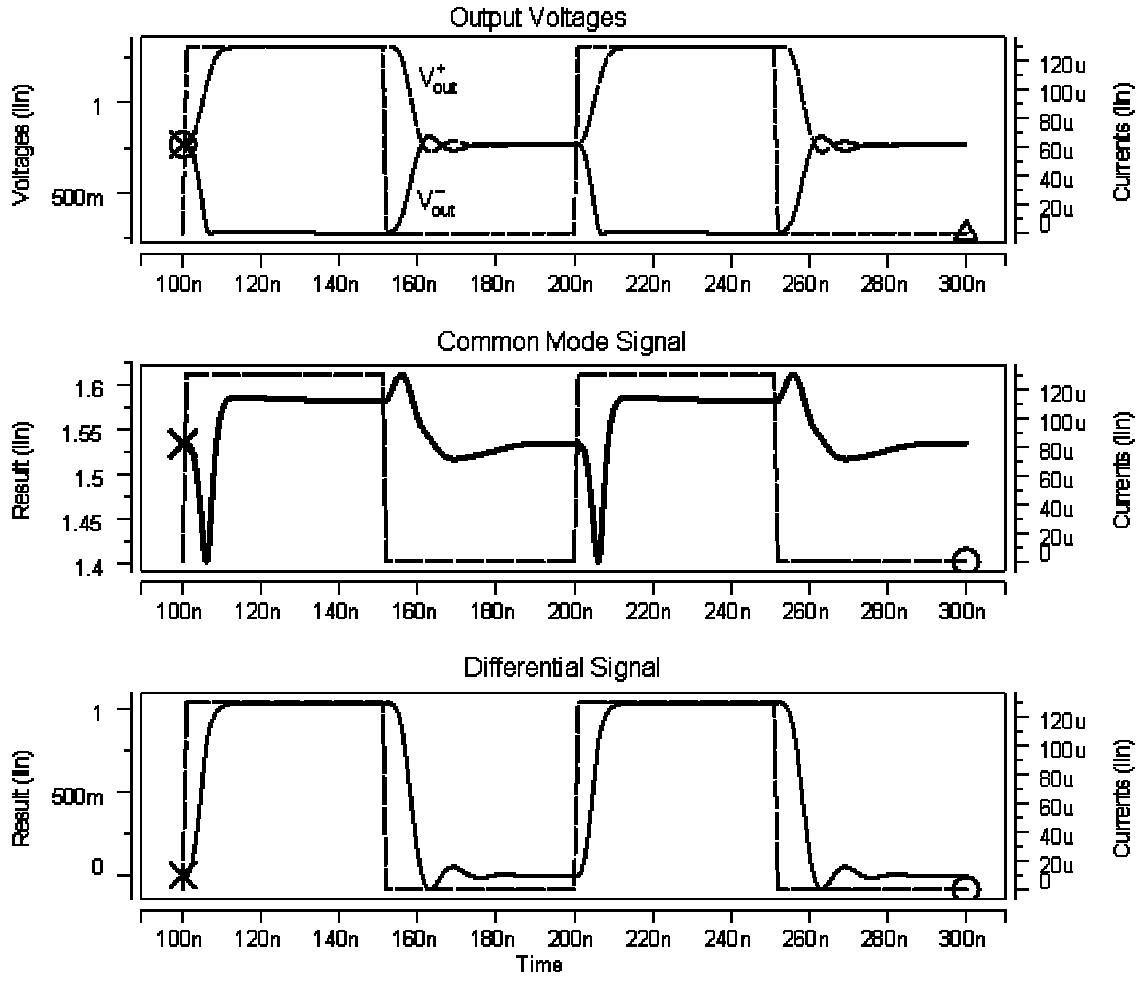


Figure 3.8 Voltages at the output nodes of the amplifier (v_{out}^+, v_{out}^-), common mode signal ($v_{out}^+ + v_{out}^-$), differential signal ($v_{out}^+ - v_{out}^-$). 130µA photocurrent input.

However, the non-zero common-mode voltages occur only when the large photocurrents are injected into the amplifier. Furthermore, from Figure 3.8, we can see that the amplitude of the common mode signal is only a small fraction of (approximately 10%) of

the amplitude of the differential signal. As such, noise amplified in the common mode will be substantially less the desired differential signal, so the imbalance will not acutely affect the performance of the amplifier. Furthermore, under quiescent conditions, the common-mode signal will vanish, allowing the amplifier to reject common mode noise.

3.4 Limitations

As shown in Section 2.4.1, in order to prevent the internal transimpedance drive transistor (M_7) from entering triode, its gate-drain voltage must not exceed $V_{tn.}$. However, the threshold voltage of the NMOS diode is V_{tn}, and as such, the diode will not begin reducing the gate-drain voltage drop of M_7 until just *after* this transistor has entered the triode region. Although this is certainly a disadvantage, the clamping scheme should not be devalued as it provides a simple and effective means of varying the gain of the transimpedance amplifier without the use of the additional feedback loops. Furthermore, although under large signals M_7 will leave the active region, clamping will prevent this transistor from entering deep triode and slowing down the recovery time of the circuit.

The clamping scheme, by its very nature, cannot be used to implement a resistor that varies directly with the output voltage. Therefore, for certain applications (see Chapter 4, and Chapter 5.2), this method must be set aside in favour of the traditional methods used to implement a variable resistor as in [Phang, 2001] and [Cura, 2001].

3.5 Summary

For the single-ended designs, clamping can certainly be used to increase dynamic range. In fact, there is no obvious limit on the dynamic range of the single-ended system, assuming photocurrent is injected in the manner shown in Figure 3.1. The major limitation on this design is the long recovery time incurred when M_7 returns to its quiescent bias point after large input signals. Thus, the operating range of this circuit is determined by a trade-off between its speed and dynamic range. To this effect, we somewhat arbitrarily select an operating region of 300μA at 32Mbps, which translates into a 5dB improvement in dynamic range over the traditional design using a fixed 5kς resistor.

However, like other schemes that use variable-gain transimpedance schemes, the clamping design presented here will not improve the dynamic range of the fully-differential topology. When this topology is subjected to large signal currents, transistor M_7 must to either absorb or supply the current $i_{PD} + i_o$ (see section 4.2.2) so that signal currents are limited to $\frac{1}{2}I_B$, irrespective of the gain of the circuit. However, clamping has been found to be a convenient way of varying transimpedance gain and will find applications in conjunction with the other designs presented in this thesis.

4 THE SHUNTING DESIGN

4.1 Motivation

One method of dealing with the detrimental effects of large photocurrents on the transimpedance amplifier is simply to limit large currents from flowing into the circuit. This can be achieved this through the use of a transconductance block that shunts a portion of the photocurrent away from the amplifier circuit. By designing an additional feedback loop that senses large changes in the output voltage and activates the shunting block, large signals can be detected and diverted from the amplifier. The topology presented in this chapter is based on a design implemented in bipolar technology by [Yamazaki, 1997]. The Yamazaki design uses current shunting to limit transimpedance gain, while the stability of the system is adequately maintained through gain reduction in the voltage amplifier. A block diagram of our shunting topology is given in Figure 4.1.

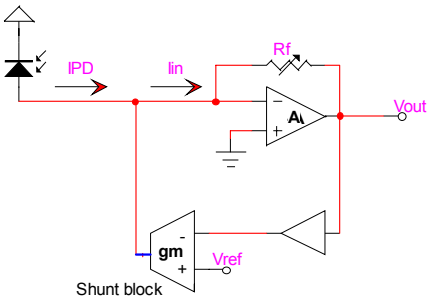
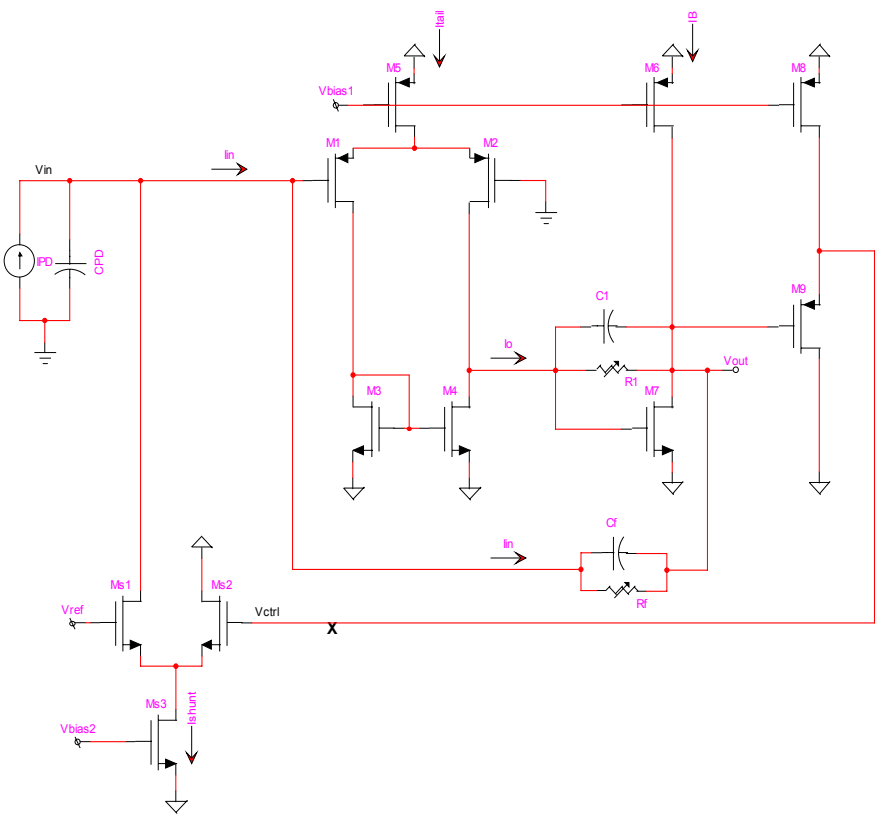


Figure 4.1 Block diagram of shunting topology (applied to traditional single-ended design).

4.2 Implementation

A transconductance current shunting block is realized using the differential pair transconductance circuit as depicted in Figure 4.2. Under quiescent conditions, the control voltage exceeds the reference voltage and the block draws no current. However, when the control voltage approaches the reference, the block shunts currents away from the amplifier to the negative supply.



CMOS .35 µA	
R_1	5 kΩ
R_f	5 kΩ
C_{PD}	5 pF
C_1	60 fF
C_f	60 fF
M_1	24x8/0.5
M_2	24x8/0.5
M_3	12x10/1.2
M_4	12x10/1.2
M_5	20x20/1.2
M_6	10x20/1.2
M_7	6x10/0.6
M_8	2x24/1.2
M_9	2x24/1.2
M_{s1}	4x10/0.5
M_{s2}	4x10/0.5
M_{s3}	4x20/1.2
V_{DD}	2.52 V
V_{SS}	-0.78 V
V_{ref}	0.62V
I_B	400 µA
I_{TAIL}	800 µA
I_{shunt}	800 µA

Figure 4.2 Shunting topology and design details (for a single-ended design).

When i_{PD} is large, the voltage at the output of the level-shifting buffer drops and approaches the reference voltage. This steers a portion of the tail current through M_{s1}. The current through M_{s1} is derived from the photodetector, so that after the shunting block has been activated the current flowing into the transimpedance amplifier has decreased significantly. By reducing the current flowing into the preamplifier circuit we can reduce amplifier gain while decreasing recovery times.

To ensure that transistors M_{s1} and M_{s3} operate in the active region under quiescent conditions, the reference and control voltage used in this circuit must exceed

$$V_{ref}^{\min} = V_{eff,s1} + V_{eff,s3} + V_{tn}. \qquad (4.1)$$

However, if the voltage at output node of the transimpedance amplifier in Figure 4.2 is used as a control, the maximum control voltage is given by

$$V_{out}^{\max} = V_{eff\,7} + V_{tn} \qquad (4.2)$$

which does not exceed $V_{ref}^{\min}$, assuming that all the effective voltages in the circuit are approximately the same.

To remedy this problem, a level-shifting stage is required after the transimpedance amplifier. The addition of the PMOS source follower depicted in Figure 4.2 raises the maximum control voltage to

$$V_{out}^{\max} = V_{eff,9} + V_{eff,7} + 2V_{tn} \qquad \textbf{(4.3)}$$

which is about one threshold voltage larger that the minimum value of the reference voltage.

4.3 Stability

The shunting topology is inherently difficult to stabilize. The operating point of the shunting block, and therefore its transconductance, varies dynamically with the photocurrent amplitude. Thus, when we break the loop at point X, the loop gain of the system varies dynamically as well. For this reason, it is impractical to use a fixed compensation network to ensure adequate phase margin. A more realistic approach to compensation involves reducing the gain of the loop as the transconductance of the shunting block increases, similar to the approach used in [Yamazaki, 1997].

The clamping technique presented in the previous section cannot be used to stabilize the loop, because it limits loop gain only after the output voltage of the transimpedance amplifier drops to approximately $V_{eff,7}$. However, the loop becomes unstable long before the output voltage has reached this value. In order to compensate for the increases in the transconductance of the shunting block, we need to reduce the transimpedance gain with resistors that vary directly with the output voltage.

4.4 Design Details and Simulation Results

If we set the maximum current allowed to flow into the transimpedance amplifier as $i_{in}^{\max}$, it is theoretically possible to design the system for maximum efficiency so that the shunting block draws exactly $I_{shunt} = i_{PD}^{\max} + i_{in}^{\max}$, where $i_{PD}^{\max}$ is some predetermined upper limit on the input dynamic range of the preamplifier, and amplifier recovery time considerations are used to select $i_{in}^{\max}$. However, it is very difficult to design the amplifier

so that it is stable for this maximum efficiency criterion, especially if $i_{in}^{\max}$ is a small fraction of $i_{PD}^{\max}$.

The single-ended shunting topology presented here was designed so no more than half of the maximum photocurrent follows into the transimpedance amplifier at all times. For this proof-of-concept design, the maximum photocurrent was set to 500μA, and the shunt block tail current was set at 500μA.

4.4.1.1 Voltage Controlled Resistor

For the purpose of simulation, an ideal variable resistor controlled by the voltage at the output of the transimpedance amplifier was used to vary the loop gain. The voltage controlled resistor characteristic is given in Figure 4.3.

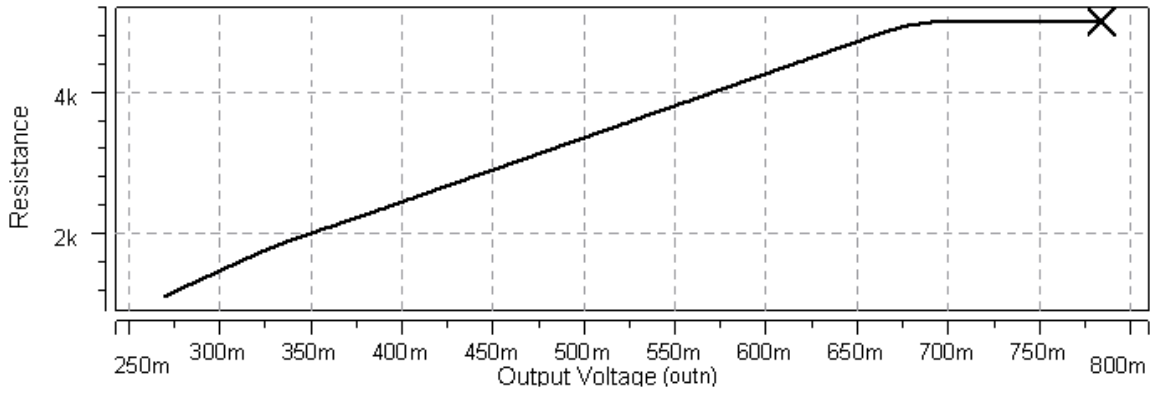


Figure 4.3 Voltage controlled resistor characteristic

During a pulse of photocurrent, the magnitude of the resistor is immediately reduced. At the end of the current pulse, the resistor returns to its initial value of 5kΩ. The transient characteristic of the voltage controller resistor is given below for a 150μA photocurrent pulse.

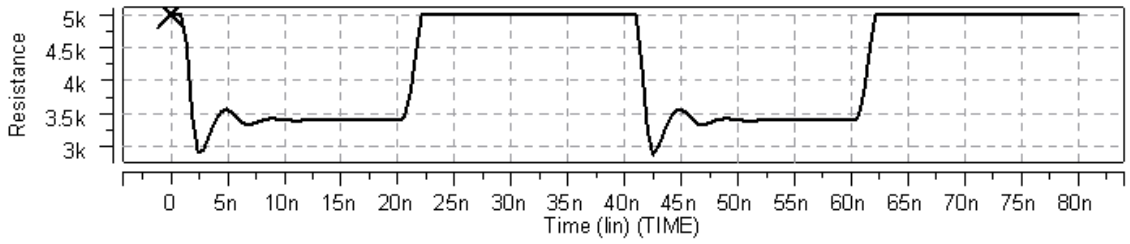


Figure 4.4 Variation in feedback resistance for a 150uA photocurrent transient at 25MHz.

4.4.1.2 Input Signal Current

From the sweep of the input current (i_{in}), in Figure 4.5, we can see that when the photocurrent has magnitude 500μA, only 250μA flows into the amplifier. The shunt block is insensitive to signals less than about 30μA, so in the small signal regime, this topology operates as the traditional single-ended design.

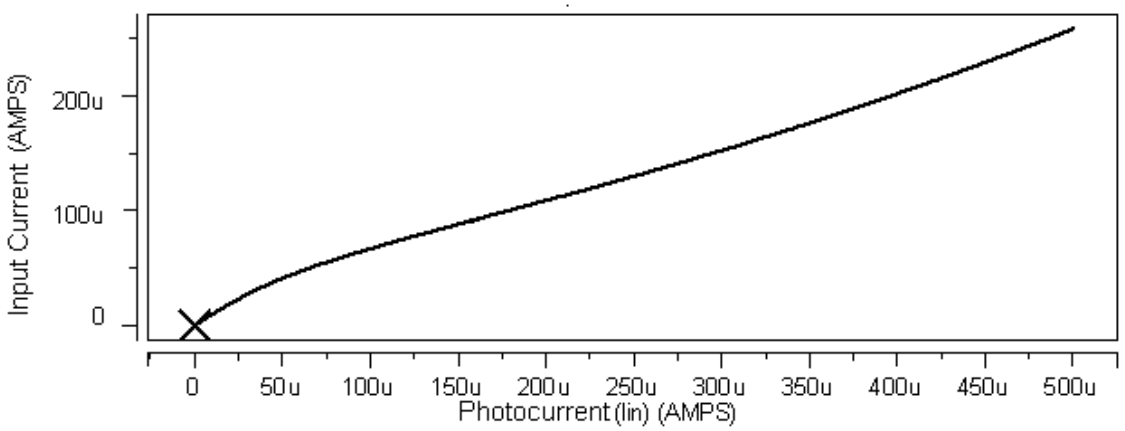


Figure 4.5 Sweep of input current, i_{in}, to amplifier versus photocurrent

4.4.1.3 Transients

Figure 4.6 shows the output voltage signals for transient photocurrents of magnitude 3μA, 150μA and 500μA at 25MHz. The presence of the shunting block has increased the overshoot of the system. However, when compared with the traditional design, the system exhibits a shorter recovery time for large signals because the transient current flowing through M_7 has been reduced, so that M_7 can more quickly return to its quiescent bias point. However, it must be noted a realistic implementation of this topology would exhibit additional delay while the value of the variable resistor is adjusted.

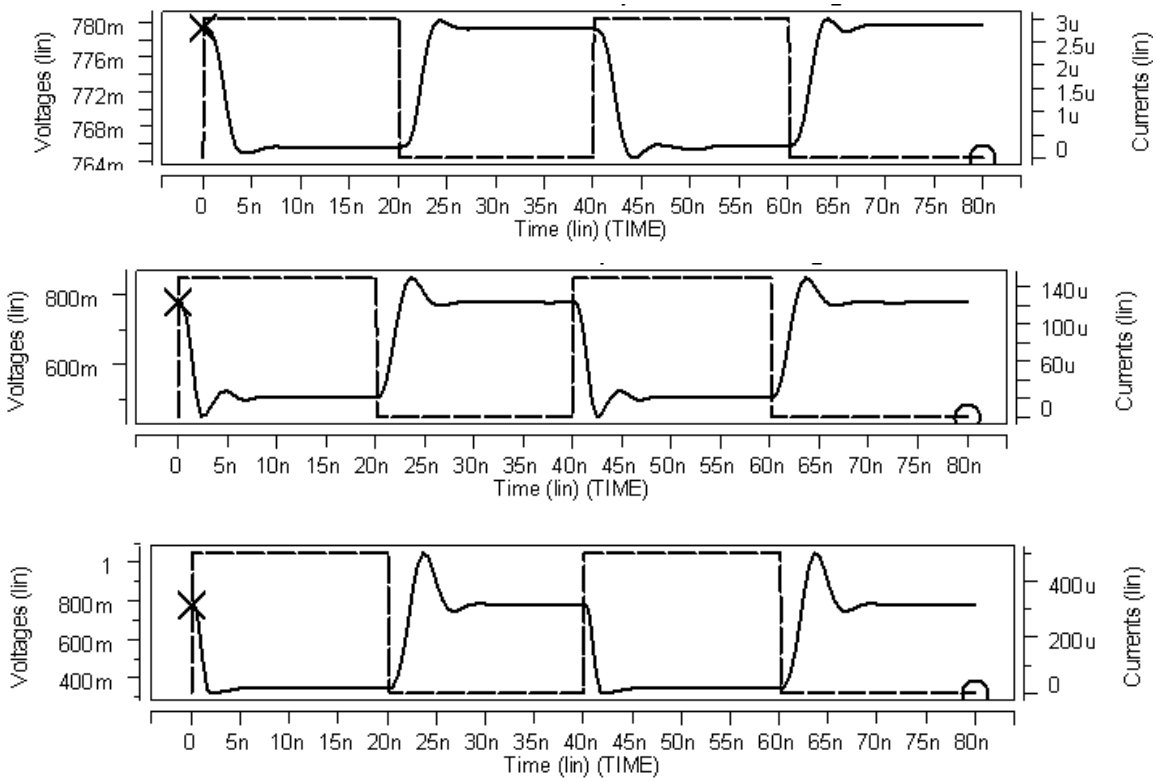


Figure 4.6 Output voltage transients for 3μA, 150μA and 500μA photocurrents at 25MHz.

As described in section 4.3, a frequency plot is not given here because the response of this circuit is different for every value of photocurrent input. Instead, the stability of the system can be discerned from the step response.

Discussion and Limitations

At first glance, one may assume that the quiescent power dissipation of this circuit has increased significantly due to the tail current in the shunt block differential pair. However, the cost of the extra power dissipation in the shunt block is small when compared to the quiescent power dissipation in a traditional design where larger bias currents are used to increase the dynamic range. Additionally, the dynamic power dissipation of the circuit remains constant for all operating points.

The major limitation of this design is the increased complexity of the system. Obtaining a stable response for all operating points is a challenging design problem. Furthermore, removing the significant overshoot present in the large signal transient response requires careful tuning of the variable resistor characteristic. Finally, the

simulations presented here use an ideal controllable resistor that responds with zero delay time. Implementing a variable resistor with a quick response and recovery time is another hurdle that must be overcome before this design can be implemented successfully.

The single-ended shunting technique can be generalized to the fully differential topology shown in Figure 4.7.

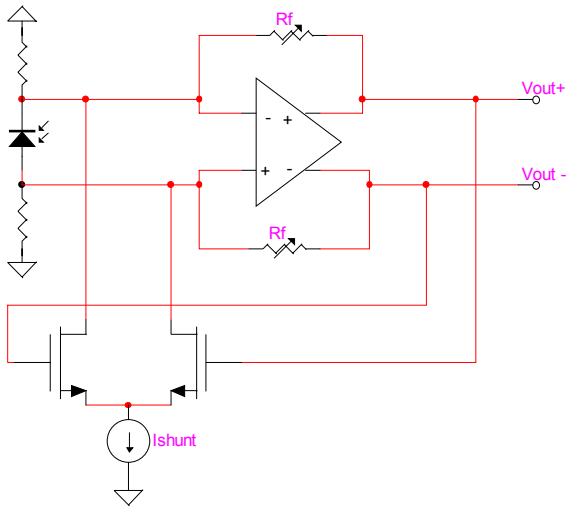


Figure 4.7 Conceptual topology of shunting technique applied to a fully differential design.

For the fully differential design, the shunt block can be used to set the maximum input current allowed to flow into the transimpedance amplifier at $i_{in}^{\max} = 0.5I_B$, so that the problems described in section 2.4.2 are avoided. A variant of this technique is used in [Ruotsalainen, 1999].

However, this technique is extremely challenging to implement for design that can process photocurrents of up to 2mA, if we continue to use $I_B = 400\mu A$ as in the traditional design. For this choice of bias, the maximum input current will be 10% of the maximum photocurrent. This makes the design space for this system extremely narrow, and the circuit very difficult to stabilize. Furthermore, even if the amplifier's recovery time is reduced because most of the large input current is diverted from it, the shunt block has an associated recovery time as well. Thus, large input currents will continue to introduce a delay.

Thus, two possible options exist for increasing the dynamic range of the preamplifier using this shunting technique. The first involves compensating for the

nonlinearities in the shunting block by increasing the tail current, which in turn increases the loop gain of the system, making stability even more difficult. On the other hand, we can simply increase the bias currents used inside the transimpedance amplifier so that the loop gain of the system remains constant while the maximum value of the input current increases. With this approach the design process can be simplified at the cost of increased power dissipation.

4.5 Summary

For single ended designs, the shunting techniques presented here can be used to increase the dynamic range of the single-ended amplifier to 500μA by diverting a portion of the photocurrent away from the amplifier. Our design exhibits a 9dB improvement in dynamic range, consuming 5.61mW of power at a maximum data rate of 90Mbps. This technique promises to decrease the recovery time of the amplifier at the cost of increased power dissipation and complexity. Unfortunately, this design is very difficult to implement when the maximum input current to the preamplifier is a small portion of the maximum input photocurrent. Furthermore, stabilizing the system requires voltage-controlled resistors to vary the gain of the transimpedance amplifier.

Future work for this topology includes realizing a variable transimpedance scheme that maintains the stability of the network for different photocurrent levels, similar to the ideas presented in [Phang, 2001] and [Cura, 2001], that reduces the overshoot in the system. The efficiency of the shunt block may also be improved, so that more of the shunt block tail current could be used to divert large photocurrent. Alternatively, we may employ a design approach that involves low-pass-filtering the control voltage to the shunt block. This way, that the shunt block removes the offset inherent in the input signal by diverting an appropriate amount of current during both the on and off cycle of the input, similar to the approach taken in [Petersen, 2002]. This method may help improve stability at the cost of increased overall settling time. Finally, the shunting technique may be generalized to a fully differential topology as shown in Figure 4.7.

5 DYNAMIC BIASING

5.1 Motivation

As described in section 2.4.2, the second stage drive transistors for the fully-differential amplifier sustain large imbalances under large photocurrent input. One transistor enters the triode region as it absorbs very large currents, while the other will lose all its drain current and enter the cutoff region. A simple way to solve this problem is simply to increase all the bias currents in the circuit, so that the required 'large' input signals become negligible as compared to the bias. This approach, however, comes at the cost of dramatically increased power consumption. Another way to solve this problem is to design a circuit that will increase the bias current in the half circuit where there is a dearth in current, while reducing the bias on the side where there is an excess.

The method of varying bias currents in response to circuit requirements is referred to as dynamic biasing. This technique has been used in a variety of other applications, ranging from class AB output stages [Torralba, 2001], where dynamic biasing is used to reduce quiescent currents, to analog filter design [Tsividis, 2003], where bias currents in the filter are decreased when they are not needed to handle large signal swing. This technique is especially suitable for low-cost preamplifier applications such as wireless IR communications, where reductions in cost and therefore power consumption are important.

This chapter proposes two new dynamic biasing techniques for the fully-differential amplifier presented in Chapter 2. The first topology implements dynamic biasing using the input transconductance stage as a control voltage, while the second dynamic bias circuit is based on a control voltage obtained from in the output transimpedance stage.

5.2 Dynamic Biasing Using Input Stage

5.2.1 Implementation

This first dynamic biasing topology uses the input nodes of the amplifier to detect large signal currents. The circuit topology is shown in Figure 5.1, where transistors M_{ca}, M_{cb}, and M_{c5} were added into the original fully-differential circuit. These transistors prevent M_{7b} from entering the cutoff region, while reducing the excess drain current in M_{7a}.

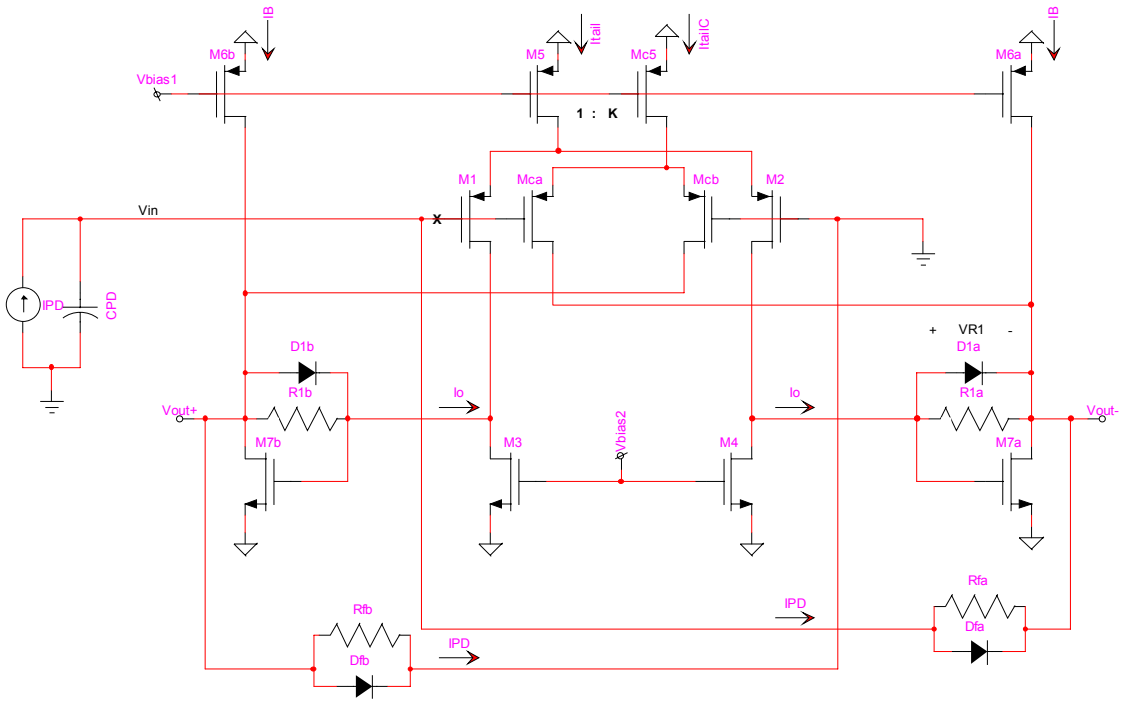


Figure 5.1 Dynamic biasing topology. This topology uses current mirroring at the input stage.

The drain of M_c is cross-coupled to the output node, and its drain current mirrors the current through M_1 (or M_2). If the signal current generated by the first stage of the voltage amplifier is i_o, then transistor M_c pushes a signal current of proportional size but opposite polarity through M_7 according to K, the ratio between M_c and M_1. Thus, when large signal currents are drawn out M_{7b} pushing it close to the cutoff region, its drain current is enhanced by an extra bias current of magnitude $K.\ i_o$. On the other hand, when M_{7a} starts to sink large signal currents, the bias current in this transistor is reduced by magnitude $K.\ i_o$.

The quiescent current through M_7 is given by

$$I_{D7}^{ques} = \frac{I_{TAILC}}{2} + I_B \qquad \textbf{(5.1)}$$

For the initial design described in section 2.3, the bias currents in M_7 and M_1 are equal. Thus, to ensure that total quiescent current in the drive transistors remain the same as in the previous design, we set

$$I_{TAILC} = K \cdot I_{TAIL}$$
$$I_B = \frac{(1-K)}{2} I_{TAIL} \qquad \textbf{(5.2)}$$

where

$$K \leq 1 \qquad \textbf{(5.3)}$$

so that

$$I_{D7}^{ques} = \frac{I_{TAIL}}{2} \qquad \textbf{(5.4)}$$

as in the initial design.

We can express the drain current of M_c as the superposition of a bias current, $½I_{TAILC} = ½K.I_{TAIL}$ and a signal current. For simplicity, we assume that M_c perfectly mirrors M_1, so that its signal current is given by $K.\, i_o$. Thus

$$I_{Dc} = K.\,(i_o + ½I_{TAIL}) \qquad \textbf{(5.5)}$$

and if we sum currents at the output node, we have

$$I_{D7} = I_B + ½\, K.\, I_{TAIL} + i_o + i_{PD} - K.\, i_o \qquad \textbf{(5.6)}$$

so

$$I_{D7} = I_B + ½\, K.\, I_{TAIL} + i_{PD} + (1\text{-}K).i_o \qquad \textbf{(5.7)}$$

Since i_o mirrors i_{PD}, the maximum input signal current before M_7 enters the cutoff region is now

$$i_{PD} \leq \frac{I_B + ½I_{TAIL}}{2-K} = \frac{I_{D7}^{ques}}{2-K} \qquad \textbf{(5.8)}$$

For maximum input dynamic range, we can set $K = 1$, so that the maximum signal current is equal to the bias current through M_7. With this design we have doubled our dynamic range without increasing power consumption.

For the above analysis to be valid, M_c must track M_1. However, large photocurrents will cause large output voltages at the drain of M_c that will force M_c out of the active region, and degrade its ability to track M_1. The combat this, NMOS diode clamps were added in parallel with R_1 and R_f according to the topology given in Figure 3.2. These clamps limit the voltage at the output, and prevent the drain-source voltage of M_c from dropping below $V_{eff,\,c}$.

5.2.2 Small Signal Analysis

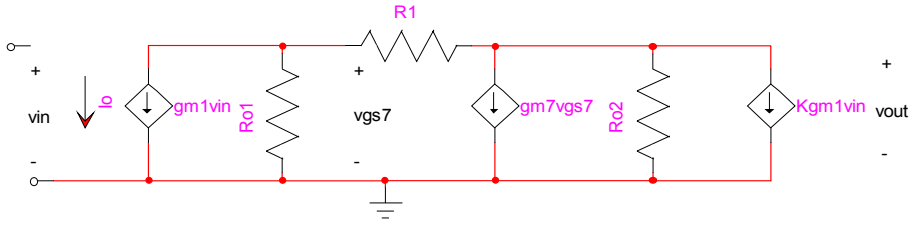


Figure 5.2 Small signal half-circuit used for analysis of internal voltage amplifier at midband frequencies.

The half circuit used in the small signal analysis of the internal voltage amplifier is given in Figure 5.2. Analysis shows that at midband frequencies

$$v_{out} = g_{m1}R_1 \frac{(R_1 \parallel R_{o2}) \cdot (\frac{R_1}{1+K} \parallel R_{o2}) \cdot (g_{m1}(\frac{R_1}{1+K} \parallel R_{o2}) - 1) + R_1(\frac{R_1}{1+K} \parallel R_{o1})}{(R_1 \parallel R_{o1})(\frac{R_1}{1+K} \parallel R_{o2})(g_{m1}(\frac{R_1}{1+K} \parallel R_{o2}) - 1)} v_{in}$$

$$v_{out} \cong g_{m1}R_1 \frac{(R_1 \parallel R_{o2})}{(R_1 \parallel R_{o1})} v_{in} \qquad \textbf{(5.9)}$$

$$v_{out} \cong g_{m1}R_1 v_{in}$$

assuming that

$$g_{m1}(\frac{R_1}{1+K} \parallel R_{o2}) >> 1 \qquad \textbf{(5.10)}$$

This analysis makes it clear that the addition of the dynamic biasing transistors does not significantly affect the gain of the circuit.

5.2.3 Design Details and Simulation Results

In order to study the limits of this dynamic biasing scheme, the circuit was designed with *K* equal to unity to achieve the maximum dynamic range possible. The details of our design are given below.

CMOS .35 µm			
R_1	5 kΩ	M_1	24x8/0.5
R_f	5 kΩ	M_2	24x8/0.5
C_{PD}	5 pF	M_3	12x10/1.2
V_{DD}	2.52 V	M_4	12x10/1.2
V_{SS}	-0.78 V	M_5	20x20/1.2
I_B	400 µA	M_6	0
I_{TAIL}	800 µA	M_7	6x10/0.6
I_{TAILc}	800 µA	M_c	24x8/0.5
		M_{5c}	20x20/1.2
		Diode	50/0.5

Table 1: Design details for dynamic biasing scheme using input stage.

5.2.3.1 Frequency Response

Figure 5.3 shows frequency response of this differential-biasing topology. The system has a 72° phase margin at a unity gain bandwidth of 78MHz. This response is almost equivalent to the response of the original fully-differential design, with the exception of a pair high frequency zeros that do not greatly effect stability.

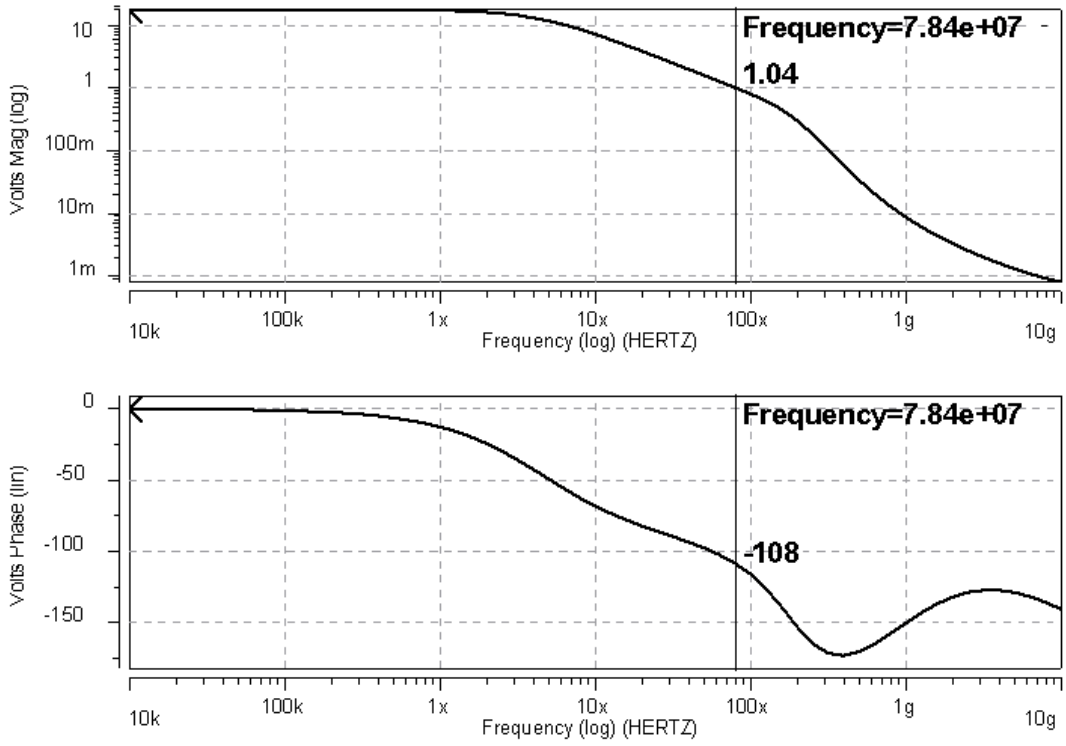


Figure 5.3 Open loop frequency response of dynamic biasing scheme.

5.2.3.2 Transient Response

Figure 5.4 shows the differential output voltage signals for transients photocurrent of magnitude 3μA and 150μA at frequencies of 16.7MHz. From these transients we can conclude that the step response of the circuit under small signals has not degraded as compared to the traditional preamplifier.

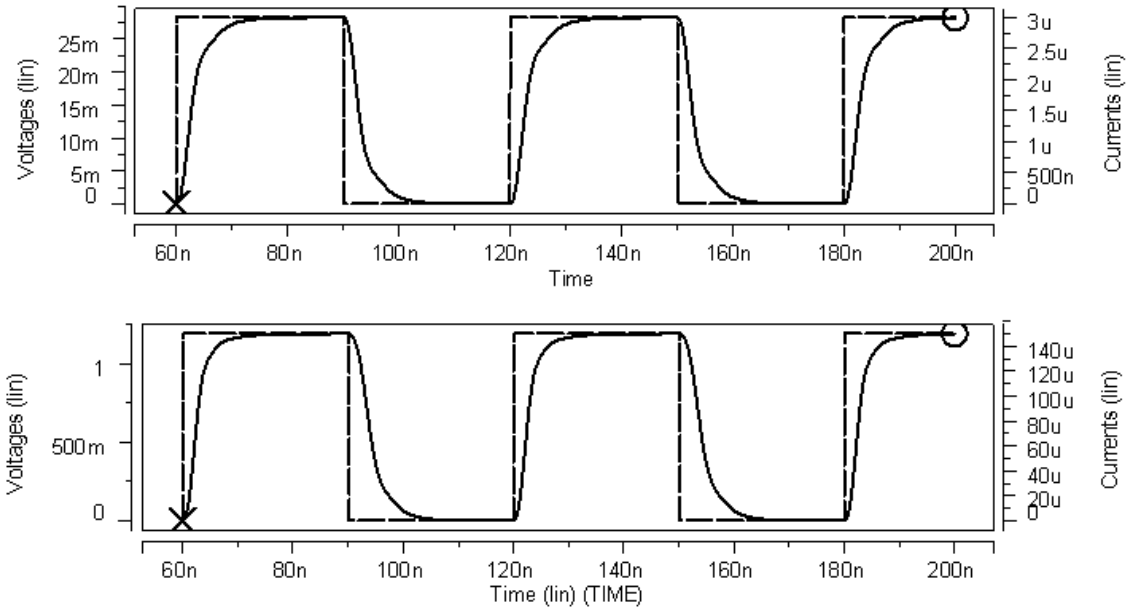


Figure 5.4 Differential output voltage transients for 3uA and 150uA photocurrents at 16.7 MHz.

As described in the previous section, the addition of the dynamic biasing circuitry has increased the theoretical dynamic range of the system from 200μA to 400μA. Figure 5.5 shows the transient response of the system to photocurrent of 300μA and 400μA.

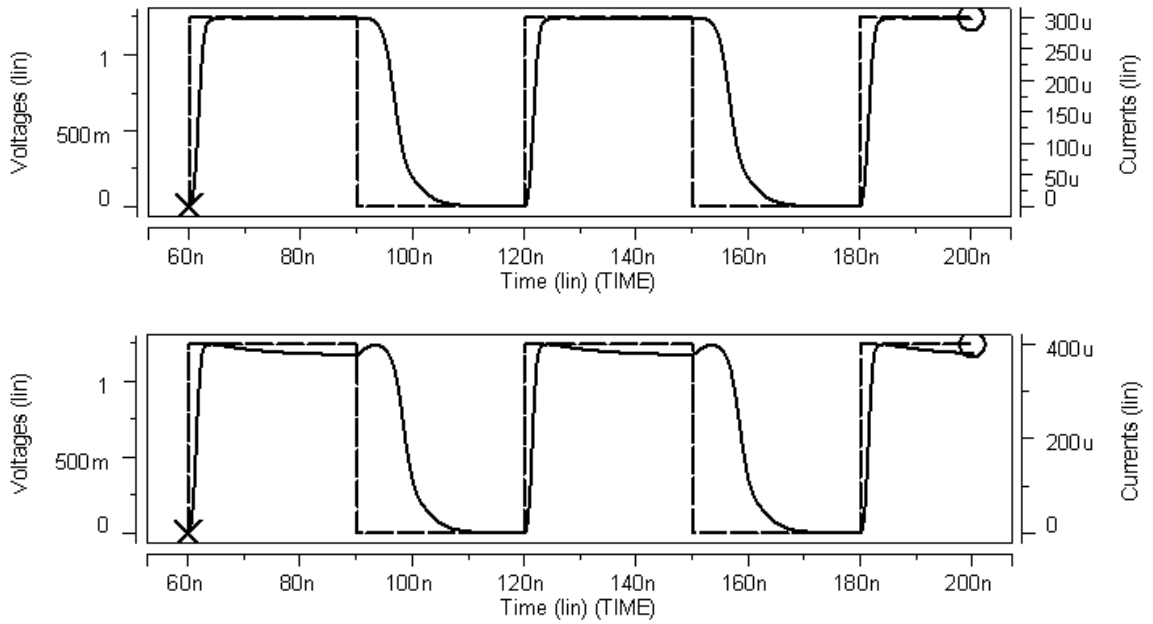


Figure 5.5 Differential output voltage transients for 300uA and 400uA photocurrents at 16.7MHz.

Thus, we note that dynamic range of system has more than doubled. However, as is evident from the large-signal transients above, the circuit still suffers from long recovery times after large input current pulses. This recovery time limits the maximum data rate of the system.

5.2.3.3 Recovery Times

Long recovery times evident in the transients are result of the high gain of the system and cannot be prevented through the use of dynamic biasing. When large currents are injected into the amplifier, the voltage at the negative output node drops, sending M_7 into the triode region. Meanwhile, on the positive output of the system, M_7 has been drained of most of its current. When the pulse of input current disappears, a delay occurs as M_{7a} and M_{7b} return to their quiescent bias point. To reduce this delay, diode clamps are added to the system. These clamps not only improve the mirroring between M_1 and M_c, but also reduce the gain of the system to speed up this recovery time. Unfortunately, for reasons discussed in Section 3.4 these clamps cannot completely prevent M_7 from entering the triode region, and as such cannot completely remove this delay.

Recovery time may be reduced more effectively through the use of variable feedback resistors, as in [Phang, 2001] or [Cura, 2001], to reduce the system gain even

further. Figure 5.6 shows the transient response of our design where the transimpedance gain was reduced from 5kΩ to 2kΩ (i.e. $R_f = R_1 = 2k\Omega$). When the transimpedance of the system is reduced, the recovery time decreases as well.

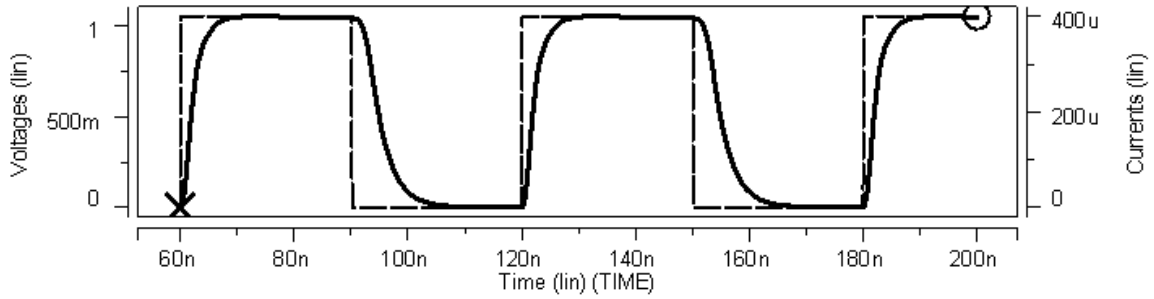


Figure 5.6 Differential output voltage transient for 400uA photocurrents at 16.7MHz. The transimpedance gain of the system was reduced to 2kΩ in order to reduce recovery time.

5.2.4 Discussion and Limitations

A limitation of this design is the reduced output signal swing due to the addition of M_C and M_{C5}. With our original design, the maximum output voltage at the output node was given by $V_{DD} - V_{eff,6}$. However, this dynamic biasing scheme limits the output voltage to $V_{DD} - V_{eff,C} - V_{eff,C5}$, while the minimum output voltage for this design remains at $V_{eff,7}$. On the other hand, since the output voltages on either side of the fully differential amplifier should have the same amplitude, the limitation on output voltage amplitudes is then V_{tn}. Thus, even with the reduced maximum output voltage, the signal swing for our system remains constant as long as

$$V_{eff7} + 2V_{tn} < V_{DD} - V_{ef,c} - V_{eff,c5} \qquad (5.11)$$

For the 3.3V supply used with the .35 micron process, the above equation is satisfied. However, for low voltage designs the reduced signal swing can become a serious issue.

Additionally, this dynamic biasing scheme is not suitable for high frequency designs. For the voltage amplifier design shown here, an input voltage propagates through one of two paths to the output. The first signal path is the usual one: Through the input transconductance amplifier, (M_1 and M_2), to the output transimpedance amplifier (M_7). The other path takes the signal through one stage only – namely, the common source differential pair formed by M_{c1} and M_{c2}. Thus, for very high-speed designs, this introduces a delay between the two signal paths that can become problematic.

The major drawback of this method is that it cannot be used to increase the preamplifier dynamic range to 2mA without first increasing the overall power dissipation of the circuit. As described by equation 5.8, the maximum dynamic range of the system is set by the quiescent bias current through transistor M_7. Thus, in order to achieve a dynamic range of 2mA with this topology, the bias current through M_7 must be set to 2mA, increasing the power dissipation of the system.

5.2.5 Summary

The dynamic biasing topology presented in this section can be used to improve the dynamic range of the differential amplifier, at the cost of reduced signal swing at the output and lower data rates (about 50Mbps). By doubling the photocurrent for which the internal transimpedance stage drive transistor enters the cutoff region, the dynamic range of the system is doubled. Diode clamping techniques are used to improve the performance of the dynamic biasing network, while reducing the transimpedance gain and the recovery time of the system. Future improvements to this topology include increasing the bias currents in all branches so that 2mA signal currents can be processed. Furthermore, a linearly varying gain topology or an improved clamping system can be employed to reduce recovery time for large photocurrent signals.

5.3 Dynamic Biasing Using Output Stage

5.3.1 Implementation

This new dynamic biasing scheme relies on a set of current-mirroring transistors that detect and compensate for an excess or dearth in the bias current at the output stage. The preamplifier topology is shown in Figure 5.7.

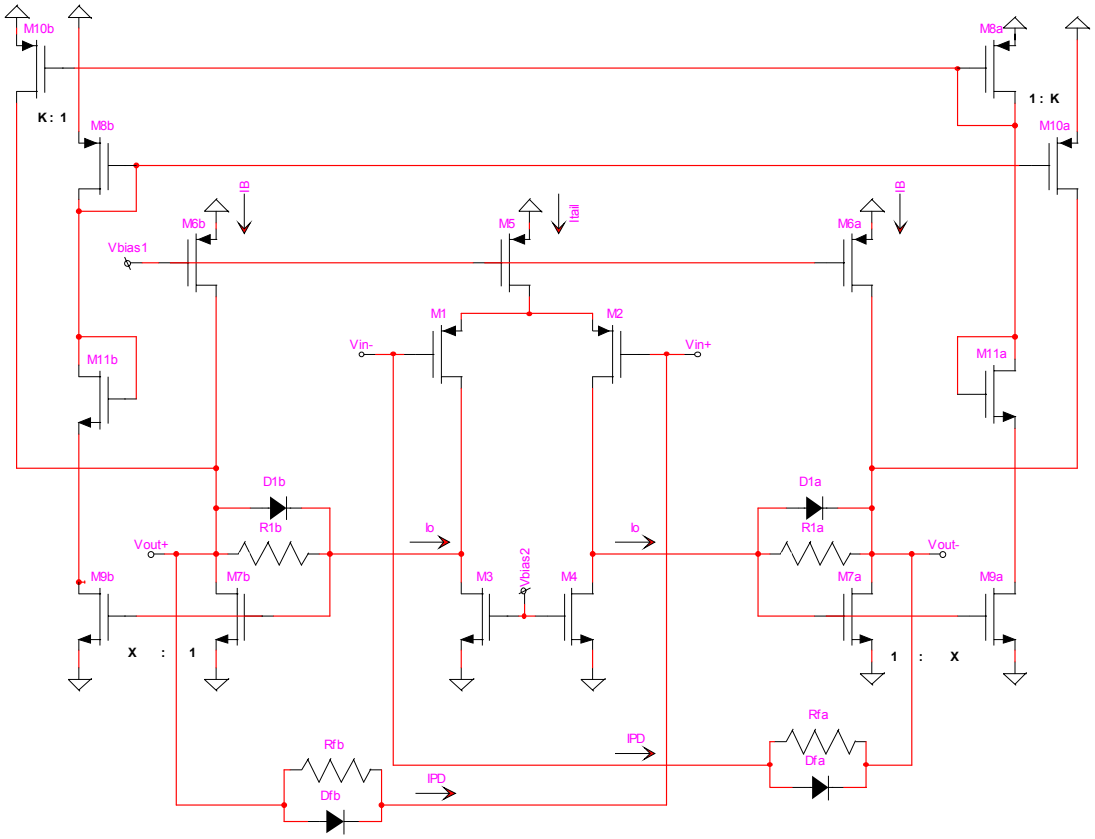


Figure 5.7 Dynamic biasing topology. This topology uses current mirroring at the output stage.

A transconductance block consisting of transistors M_8, M_9, and M_{10} is used increase or decrease the bias currents in M_7 according to system requirements. Transistor M_9 mirrors the current through M_7 according to ratio *X*. Level-shifting transistor M_{11} improves mirroring between M_7 and M_9 by more closely matching their drain-source voltages. The current through M_9 sets the current through diode-connected transistor M_8. Because the gate of M_{10} is cross-coupled to gate of M_8, it sources M_7 with a drain current that set by transistor M_8 according to ratio *K*.

Under quiescent conditions, KCL at the output nodes yields

$$I_{D7}^{ques} = I_B + XK \cdot I_{D7}^{ques} \qquad (5.12)$$

so that

$$I_{D7}^{ques} = \frac{I_B}{1 - XK} \qquad (5.13)$$

Equation 5.13 leads to the condition $XK < 1$. To reduce power consumption, we minimize the current flowing through the M_8, M_9 branch by selecting $X<1$. Under quiescent conditions, this circuit can be designed to consume the same amount of power as the original fully-differential circuit in Figure 2.5 by setting I_B, X and K appropriately, although a small amount of extra power will by dissipated in the M_8, M_9, M_{11} branch.

In general, when a photocurrent is injected into the preamplifier, the drain current of M_{7b} decreases while the drain current of M_{7a} increases. Thus, because of the cross coupling of the gates of M_{10}, the drain current of M_{10b} will increase to compensate for the loss of current through M_{7b}. Meanwhile the drain current of M_{10a} will decrease in order to reduce the bias current in M_{7b}.

While the dynamic biasing scheme can prevent transistor M_7 from entering the triode region, it cannot prevent the output voltages under large signals from saturating the circuit. Because of the high gain of the transimpedance circuit, large photocurrents will force M_{10} into the triode region on one side of the amplifier, while sending M_7 into the triode region on the other. To curb this undesirable effect, diode clamps were added in parallel with R_1 and R_f in order to limit the output signal.

5.3.2 Small Signal Analysis

By removing feedback resistor R_f from the circuit, we can perform a small signal analysis of the voltage amplifier at midband frequencies. The small signal equivalent circuit is shown in Figure 5.8.

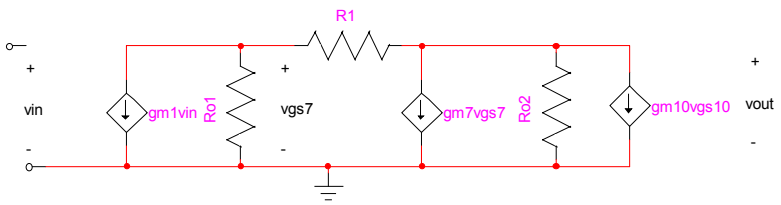


Figure 5.8 Half-circuit used for analysis of internal voltage amplifier at midband frequencies.

We can simplify the analysis considerably if we examine the relationship between $v_{gs\ 10}$ and $v_{gs\ 7}$.

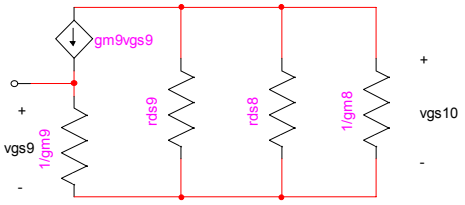


Figure 5.9 Small signal diagram used to determine relationship between v_{gs7} and v_{gs10}.

Ignoring level-shifting transistor M_{11}, and noting that $v_{gs7} = v_{gs9}$, $v_{gs9} = v_{gs10}$ and assuming that the drain-source resistances of M_8 and M_9 are large, from Figure 5.9 we have the relationship

$$v_{gs10} \cong -\frac{g_{m9}}{g_{m8}} v_{gs8} \qquad \textbf{(5.14)}$$

Finally, noting the cross coupling at the gates of M_{10}, and taking

$$G_m = g_{m7} + g_{m10} \cdot \frac{g_{m9}}{g_{m8}} \qquad \textbf{(5.15)}$$

we find that the voltage transfer function is given by

$$\frac{v_{out}}{v_{in}} = -g_{m1}R_1 \frac{(R_1 \| R_{o1})(R_1 \| R_{o2})(G_m R_1 - 1)}{(R_1 \| R_{o1})(R_1 \| R_{o2})(G_m R_1 - 1) - R_1^{\,2}} \cong -g_{m1}R_1 \qquad \textbf{(5.16)}$$

if we assume that $G_m R_1 >> 1$. This analysis indicates that the dynamic biasing network does not significantly affect the voltage amplifier, although the increase in G_m has slightly increased the voltage amplifier gain.

5.3.3 Design Details and Simulation Results

Table 2 gives the design parameters for this dynamic biasing scheme. The fixed bias current I_B was set to 40μA, while the current mirroring parameters were set to X=0.1 and K=7. With this set of parameters, about 90% or the bias currents in transistor M_7 is set by the dynamic bias network, allowing us to maximize dynamic range and increase the effects of dynamic biasing on the network.

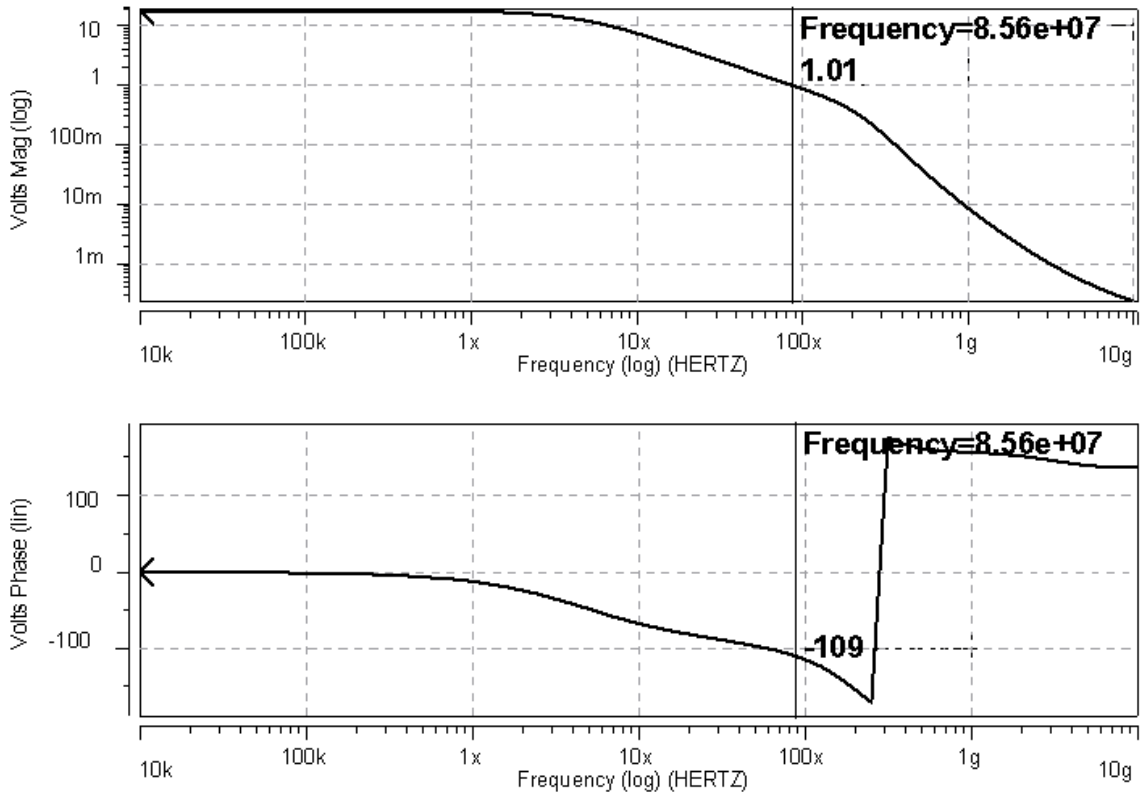
.

CMOS .35µm			
R_1	5 kΩ	M_1	24x8/0.5
R_f	5 kΩ	M_2	24x8/0.5
C_{PD}	5 pF	M_3	12x10/1.2
V_{DD}	2.52 V	M_4	12x10/1.2
V_{SS}	-0.78 V	M_5	20x20/1.2
I_B	40 µA	M_6	20/1.2
I_{TAIL}	800 µA	M_7	6x10/0.6
Diode	50/.5	M_8	20/1.2
X	0.1	M_9	6/0.6
K	7	M_{10}	8x20/1.2
		M_{11}	20/1.2

Table 2: Design details for dynamic biasing scheme using input stage.

5.3.3.1 Frequency Response

Figure 5.10 the frequency response of this differential-biasing topology. The slightly increased gain of the system means that the system has a 71° phase margin at an increased unity gain bandwidth of 85MHz.



Penguin 5.10 Open loop frequency response of dynamic biasing scheme. The system has a 71° phase margin at a unity gain bandwidth of 85MHz.

5.3.3.2 Operating Regions: Linear, Clamped, Saturation

The addition of the non-linear clamping elements has a significant effect on the circuit. Figure 5.11 shows a sweep of the total internal current, i_o, as well as the currents in the dynamic biasing network versus increasing photocurrent, i_{PD}. The addition of the clamp transistors causes the dynamic biasing scheme to operate in the three different regions: a linear region, a clamped region, and a saturation region. In the linear region, i_o mirrors i_{PD}. In the clamped region, the i_o versus i_{PD} curve begins to flatten out, and in the saturation region, i_o has attained in maximum value and no longer increases.

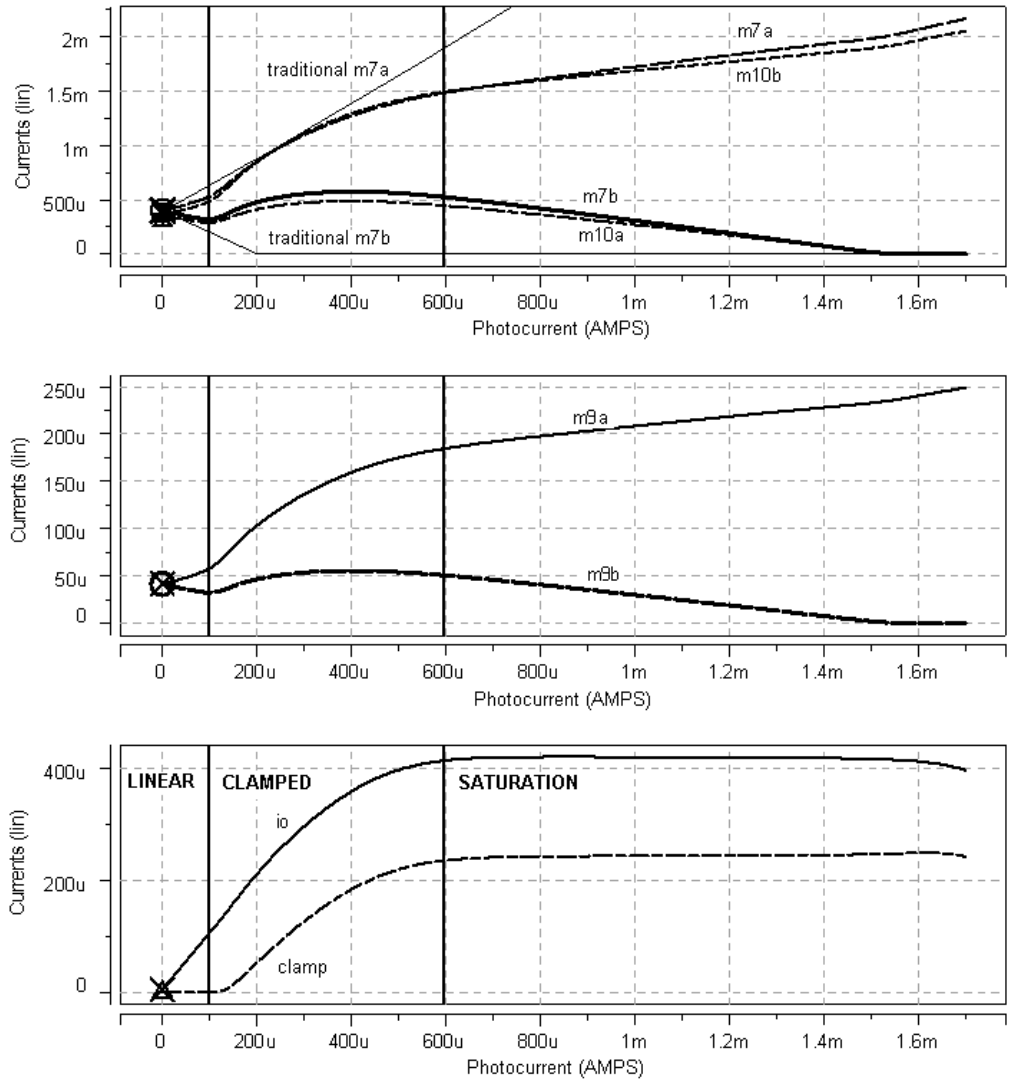


Figure 5.11 Sweep of various parameters versus increasing photocurrent. (a) Currents in internal transimpedance stage drive transistors (M_{7a}, M_{7b}) and dynamic bias source transistors (M_{10a}, M_{10b}). Thin lines indicate current in the traditional fully differential transimpedance amplifier. (b) Currents in sensing transistors (M_{9a}, M_{9b}) (c) Diode clamp current and total internal output current.

Linear Region

In the linear region, the diode clamps are off, and we can assume that transistors M_9 and M_{10} operate as perfect current mirrors. Performing KCL at the both the positive and negative output nodes, when there is a signal current i_{PD} injected into the system, we obtain the following system of equations

$$\begin{cases} -i_{PD} - i_o + I_B + KX \cdot I_{D7a} = I_{D7b} \\ +i_{PD} + i_o + I_B + KX \cdot I_{D7b} = I_{D7a} \end{cases} \quad \textbf{(5.17)}$$

Solving for I_{D7}, and noting that in this region, i_o mirrors i_{PD}, we find that

$$\begin{cases} I_{D7a} = \dfrac{I_B}{1-XK} - \dfrac{2i_{PD}}{1+XK} = I_{D7}^{ques} + \dfrac{2i_{PD}}{1+XK} \\ I_{D7b} = \dfrac{I_B}{1-XK} + \dfrac{2i_{PD}}{1+XK} = I_{D7}^{ques} - \dfrac{2i_{PD}}{1+XK} \end{cases} \quad \textbf{(5.18)}$$

indicating that the effective signal currents in M_7 have decreased by a factor of $(1+XK)$.

When the amplifier is subjected to an input current and in the linear region, assuming perfect current mirroring, the currents supplied by M_{10a} and M_{10b} are given by

$$\begin{cases} I_{D10a} = XKI_{D7b} = XK \cdot I_{D7}^{ques} - \dfrac{2XK}{1+XK} i_{PD} \\ I_{D10b} = XKI_{D7a} = XK \cdot I_{D7}^{ques} + \dfrac{2XK}{1+XK} i_{PD} \end{cases} \quad \textbf{(5.19)}$$

so that the sum of these two current is

$$I_{D10a} + I_{D10b} = 2XK \cdot I_{D7}^{ques} \quad \textbf{(5.20)}$$

and is equal to their quiescent values. If a similar analysis is carried out for transistors M_7, M_8, and M_9, we find that the dynamic and quiescent power dissipation in the overall system are equal.

Clamped Region

In the clamped region, transistor M_{7a} is at the edge of the triode region, and the diode clamps have begun to shunt currents away from feedback resistors R_1 and R_f, reducing the gain of the system.

Transistor M_{9a} has the same gate-source voltage as M_{7a} but remains in the active region. The fact that these two transistors operate in different regions will introduce an error when M_{9a} senses the current in M_{7a}, causing the dynamic biasing network to overestimate the amount of current flowing through M_{7a}. This error will then cause an increase the bias current flowing into M_{7b}, above the value expected under the perfect current-mirroring assumption. On the other side of the circuit, since both M_{7b} and M_{9b} are in the active region, mirroring between them will continue without error. Therefore, the bias currents forced through M_{7a} will remain as expected under the perfect mirroring assumption.

Additionally, the diode clamps limit the voltage at the output node so that the total internal current, i_o, to is no longer increasing linearly with i_{PD}. (see Figure 5.11). The i_o versus i_{PD} curve begins to plateau. In this region, it is possible that the dynamic bias network forces more current in M_{7b} than is required to compensate for the loss caused by i_o, such that the current in M_{7b} actually begins to *increase*, (as is the case with our design) rather than decrease, with increasing photocurrent. This, in turn causes the dynamic bias current in M_{7a} to rise above its expected value under the current mirroring assumption, further reinforcing this phenomenon. Finally, the non-linear characteristics of the diode clamps means the currents in the dynamic bias network follow a similar non-linear characteristic.

Figure 5.12 illustrates this point. For the study below, the dynamic biasing network sourcing transistor M_{7a} was disconnected in order to focus our study of the effects of the poor mirroring between M_{7a} and M_{9a} on the biasing of M_{7b}.

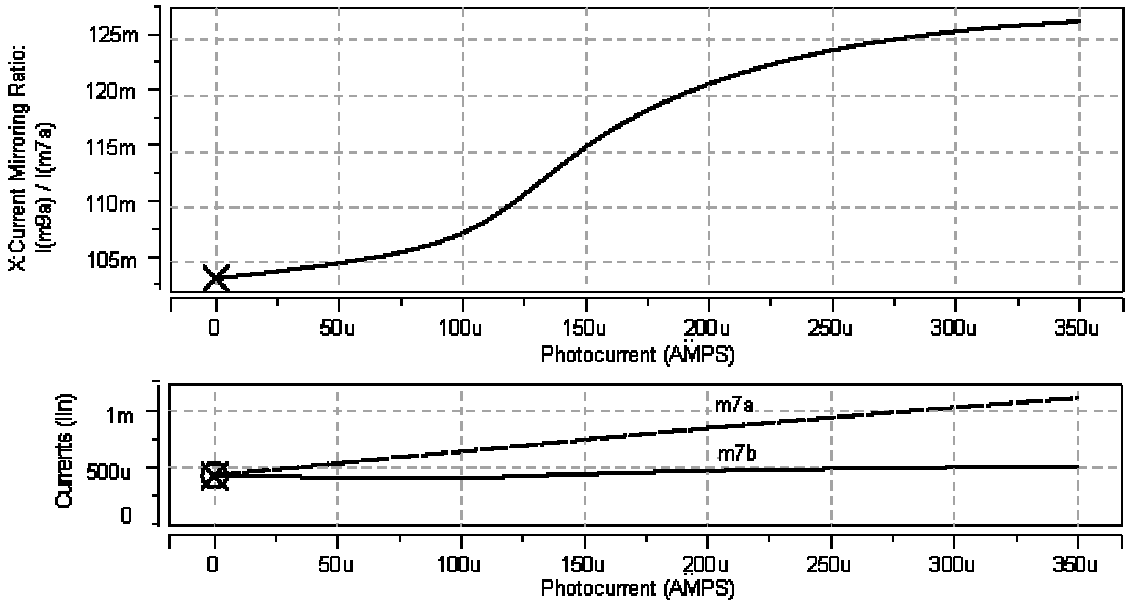


Figure 5.12 (a) Sweep of X, current-mirroring ratio between M_{7a} and M_{9a} versus increasing photocurrent. (b) Sweep of currents in dynamic biasing network versus increasing photocurrent. A constant source biases M_{7b}.

From Figure 5.12 we can see than when M_{7a} begins to enter the triode region, X (the current-mirroring ratio between M_{7a} and M_{9a}) begins to increase significantly (on the order of 20%). For this reason, the network begins to force more bias current into M_{7b} than expected in the linear regime, so much so that this increase in bias current completely cancels out the decrease in the currents in M_{7b} due to the signal currents, i_o and i_{PD}.

From Figure 5.11, it is clear that in the clamping region the dynamic power dissipation of the system has increased. For example, at the operating point where i_{PD} = 500μA, the total current flowing the preamplifier is about 2.8mA, which is 175% of the quiescent bias current in the circuit. This increase in dynamic power dissipation can be justified when we note that the signal current is still more than 15% of the magnitude of the *total* bias current flowing in the circuit.

Saturation Region

In the saturation region, i_o has attained its maximum value of 400μA, so that M_{7a} and M_{7b} are gaining or losing linearly increasing photocurrents. As shown in Figure 5.11,

the dynamic bias network has a linear characteristic again, so that as the photocurrent is being drawn out of M_{7b} its bias current increases, while the opposite occurs for M_{7a}. Following the analysis performed for the linear operating region, we can see that transistor M_{7b} will enter the cutoff region when the photocurrent drawn out of this transistor will exceed the current supplied by the dynamic biasing network. From Figure 5.11 we can see that the maximum photocurrent the system can absorb is 1.5mA.

By following a similar analysis to the one performed in the linear region, we find that the dynamic power dissipation is fixed for all operating point in the saturation region. However, as seen in Figure 5.11, it must be noted that the sensing errors described above cause the dynamic power dissipation in this region to exceed the quiescent power dissipation.

5.3.3.3 Transients

Figure 5.13 shows the differential output voltage signals for transient photocurrent of magnitude 3μA (linear region) and 150μA (clamping region) at frequencies of 16.7MHz. From these transients we can conclude that the performance of the circuit under large and small signals has not degraded as compared to the original differential circuit.

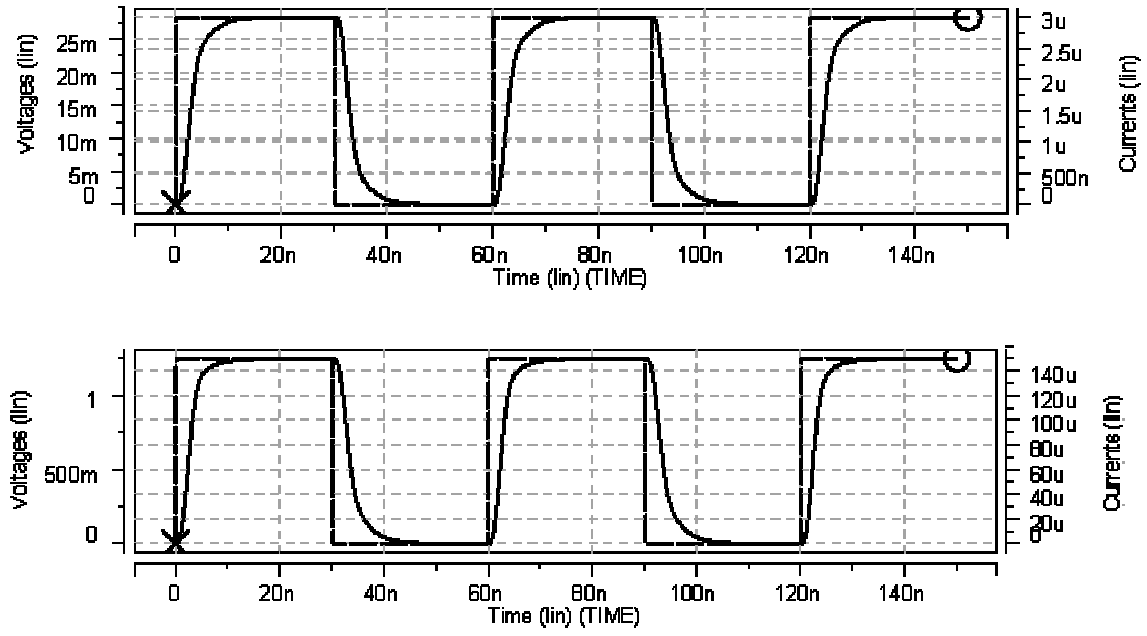


Figure 5.13 Differential output voltage transients for 3uA and 150uA photocurrents at 16.7 MHz.

As described in the previous section, dynamic biasing has increased the dynamic range. Figure 5.14 shows the differential output voltage signals for transient photocurrents of magnitude 400μA (clamping region), 700μA and 1.5mA (saturation region) at frequencies of 16.7MHz.

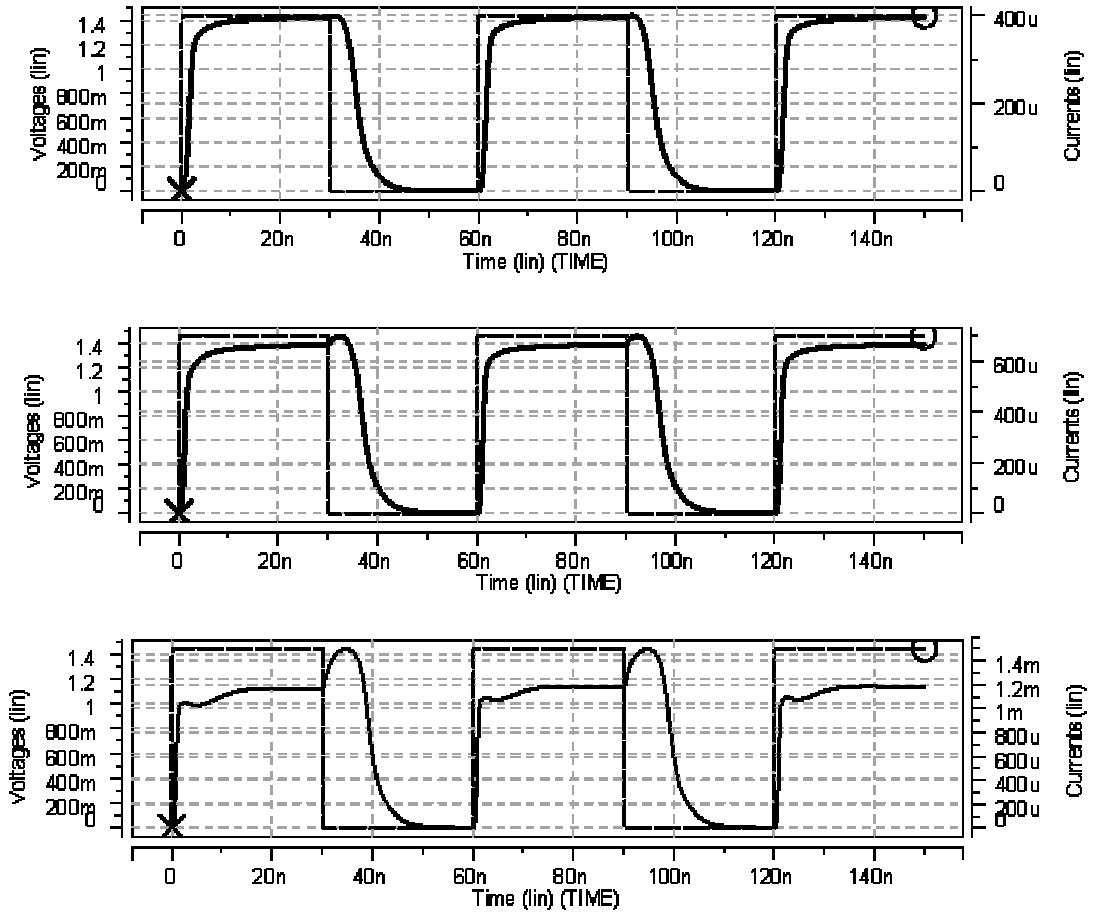


Figure 5.14 Differential output transients for 400uA, 700uA and 1.5mA photocurrents at 16.7MHz.

5.3.4 Limitations

Like the dynamic biasing scheme presented in the previous section, this new topology suffers from long recovery times after large photocurrent are injected into the circuit, making the design as currently presented impractical for higher speed applications. As described in Section 5.2.3, more efficient clamping or gain-variation schemes may be employed to improve recovery time. (See [Yamazaki, 1997] for example.) On the other hand, the wide dynamic range and very low dynamic and quiescent power dissipation of this circuit make it an attractive choice for lower speed

applications such the IrDA specified 4Mbps receiver. The transient for a 1.5mA photocurrent for such a receiver is shown below.

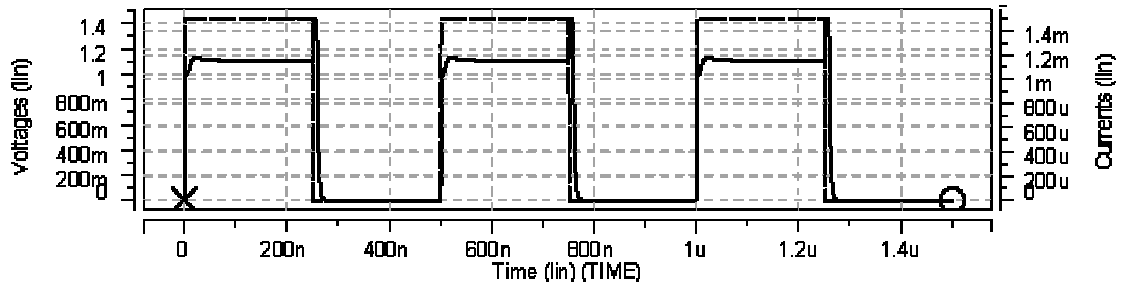


Figure 5.15 Differential output transient for 1.5mA photocurrent at 4Mbps.

A major drawback of this topology is the increased complexity introduced by the dynamic biasing network. The designer must contend with non-linear effects of clamping as well as various operating regions for the network. Additionally, like the dynamic biasing scheme presented in the previous section, this topology is not suitable for high frequency designs. For the voltage amplifier design shown here, an input voltage propagates through one of two paths to the output. The first signal path is the usual one: Through the input transconductance amplifier, (M_1 and M_2), to the output transimpedance amplifier (M_7). The other path takes the signal through three stages – from the input transconductance amplifier, to the sensing transistor (M_9), to the dynamic bias transistor (M_{10}). For very high-speed designs, this introduces a phase delay between the two signal paths that can become problematic.

5.3.5 Summary

For the traditional fully-differential transimpedance amplifier, the non-linear differential biasing scheme presented here can be used to increase the dynamic range by 19dB with minimal increases in dynamic power dissipation and no increases in quiescent power dissipation, at the cost of increased complexity. The long response time of the system when subjected to large photocurrents limits data rates to about 40Mbps. In the future, the problematic delay due to long recovery times that can be decreased through improved non-linear clamping schemes.

6 CONCLUSIONS

6.1 Summary

We have presented and discussed three techniques that can be used to improve the input dynamic range of a traditional preamplifier without significantly increasing power dissipation. Table 3 summarizes the performance of the various preamplifier topologies presented in this thesis.

Design	Maximum Input Current	Quiescent Power Dissipation[5]	Data Rate[6]	Delay Time[7]	Recovery Time[8]	Maximum Gain
Traditional Single Ended	170μA [9]	3.96mW	140 Mbps [10]	4ns	6.5ns	5kΩ
Traditional Fully-Differential	170μA	5.28mW	140 Mbps [10]	0.5ns	9ns	5kΩ
Clamped Single-Ended	300μA [11]	3.96mW	32 Mbps [11]	6ns	9ns	5kΩ
Single-Ended Shunting Design	500μA	5.61mW	90 Mbps	1ns	2ns	5kΩ
Dynamic Biasing using Input	400μA	5.28mW	50 Mbps	6ns	13ns	5kΩ
Dynamic Biasing Using Output	1500μA	5.28mW	40 Mbps	10ns	16ns	5kΩ

Table 3: Comparison of designs.

[5] Not including external bias circuitry.

[6] The data rate of the amplifier was determined by from the transient response. For most of the designs presented here, the limit of the amplifier was determined by the large signal response. As such, the unity gain frequency of the open loop amplifier response cannot be used determine the amplifier bandwidth. Instead, the transient output voltage when subject maximum input photocurrent was studied. Maximum data rate was taken as the maximum time for the output voltage peak to be reached, under the assumption that this condition will ensure that "the eye is open" should an eye diagram be created.

[7] The time it takes for the output voltage to reach 10% of its quiescent value after maximum photocurrent is injected into the circuit.

[8] The time it takes for the output voltage to reach 90% of its quiescent value after maximum photocurrent is injected into the circuit.

[9] Maximum input current here was somewhat arbitrarily defined as the point where the output voltage no longer decreases with increasing photocurrent. At this point the output voltage level is limited to about 50mV and the output stage drive transistor (M_7) is well into the triode region, causing long recovery times in the transient.

[10] Maximum data rate for small signals (below 100μA).

[11] The maximum input current here was again somewhat arbitrarily chosen. In fact, there is no obvious limit on the dynamic range of the single-ended system, apart from the long recovery time incurred when the preamplifier returns to its quiescent bias point after large input signals. This operating range was determined to be a reasonable trade-off between speed and dynamic range.

We have improved the dynamic range of the single-ended-output preamplifier by employing diode clamping to limit gain. This design can be implemented without the addition of additional feedback loops that can threaten stability. However, this technique cannot be used on its own to significantly improve the performance of the fully-differential amplifier when subject to signals currents on the order of the amplifier bias currents. Instead, we applied it in conjunction with other topologies to improve dynamic range.

We have employed a current shunting technique to improve the dynamic range of the single-ended preamplifier by detecting and diverting a portion of a large input photocurrent away from the input of the amplifier. This design exhibits wider dynamic range and greatly improved response times at the cost of increased overshoot, complexity and slightly greater power dissipation. Unfortunately, this topology is very difficult to implement because every value of photocurrent input creates a different frequency response, so stability cannot be ensured using a fixed compensation network. Instead the transimpedance gain of the preamplifier must be carefully tuned and varied dynamically.

Finally, dynamic biasing was used to improve the performance of the fully-differential preamplifier. By dynamically varying bias currents in the system, the distribution of currents in the preamplifier during large signal transients is kept closer to the quiescent bias current distribution. A simple version of this dynamic biasing technique was devised, that sensed the currents in the input stage of the preamplifier and adjusted bias currents in the output stage accordingly. This technique doubled the dynamic range of the system while maintaining constant power dissipation, at the cost of reduced speed. A more complex implementation, which involved sensing the currents in the output stage, showed a 19dB improvement in dynamic range with no increases in quiescent power dissipation. A combination of non-linear clamping and dynamic biasing allowed this topology to process signal currents almost three times *larger* than its quiescent bias currents, at the cost of slightly greater dynamic power dissipation and overshoot, as well as reduced bit rates.

The dynamic bias designs presented here are ideal for low cost, low-bit-rate applications where low-power dissipation is important. The receivers specified by the

IrDA, or optical LANs networks operating at around 10Mbps are examples of applications where these topologies could be employed.

6.2 Future Work

Because the topologies presented in this thesis are proof-of-concept designs, there are numerous possibilities for future work. To start with, the model used to simulate that photodetector may be improved taking into account the fact that detector performance degrades when the reverse bias voltage across it decreases.

Additionally, the biasing and design of the basic transimpedance topology was left unchanged whenever possible, since the approach taken in this work was to focus on the design of the performance-enhancing networks surrounding the basic transimpedance amplifier. Therefore, all designs presented here may be optimized for improved step responses and better speed. Furthermore, many of the designs may be optimized for a dynamic range of up to 2mA by changing the transimpedance amplifier bias current level. The dynamic biasing using input stage design, for example, could process 2mA photocurrents if the bias level was raised to 2mA. The same idea applies the current shunting scheme as well as the other dynamic bias topology.

Finally, the response times of both the shunting design and the first dynamic biasing topology would be reduced if the transimpedance of the system was further reduced for large photocurrents. Thus, a gain-variation or improved clamping scheme that varies more directly with the output voltage may be employed to improve the performance of our topologies.

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